Virtex-6 FPGA: Built-In Synchronous FIFO Reset and Input Logic Reset

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Customer Notification – For Your Information

Overview

Thank you for designing with the Xilinx Virtex®-6 family of devices. The purpose of this notification is to inform Xilinx customers of corrections to the described behavior of specific function blocks within the Virtex-6 FPGA. The affected function blocks include the built-in synchronous FIFO and the input logic registers.

Description

The following describes the recommended usage or actual behavior for the built-in synchronous FIFO and input logic registers.

Built-in Synchronous FIFO Reset

When the built-in FIFO is used in synchronous mode (EN_SYN=TRUE), a design must synchronize the negative edge of RESET to the RDCLK or WRCLK for correct behavior of the FIFO flags after the first write.

For details and workarounds, see Answer Record 41099 http://www.xilinx.com/support/answers/41099.htm.

Note: Any other configuration of the built-in FIFO (EN_SYN=FALSE) does not require this RESET synchronization.

Input Logic Reset Using GSR

The global set/reset (GSR) event from the FPGA configuration sequence or STARTUP_VIRTEX6 primitive does not always initialize ILOGIC input registers (IFF, IDDR, and ISERDES) to zero using the INIT=0 attribute.

If the application requires the input registers to be initialized to zero, then a separate reset using general interconnect must be implemented.

Note: GSR initialization of the input logic registers to a one (using the INIT=1 attribute) works as expected.

Products Affected

This notice applies to all Virtex-6 LXT, SXT, HXT, and CXT FPGAs. The products affected include all standard part numbers and specification control document (SCD) versions of the standard part numbers.

Key Dates

These changes are effective upon this PCN release.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support http://www.xilinx.com/support/techsup/tappinfo.htm.

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Additional Documentation

Virtex-6 FPGA Documentation:

http://www.xilinx.com/support/documentation/virtex-6.htm

Xilinx Answer Record Database:

http://www.xilinx.com/support/answers/

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/18/11	1.0	Initial release.

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