7 Series FPGAs Packaging and Pinout

Advance Specification

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/11	1.0	Initial Xilinx release.
04/06/11	1.1	Removed the SBG324 package from the entire document. Added three Kintex-7 devices: XC7K355T, XC7K420T, and XC7K480T. Updated disclaimer and copyright on page 2. Updated package size of FF1156 in Table 1-1. Updated DXP_0, DXN_0 in Table 1-9. The Table 2-2 single ASCII device files have been updated for both the XC7K70T and XC7K160T. All ASCII TXT files and the overall ZIP file have been updated on the web. Updated the XC7K70TFBG676 figures: Figure 3-13, Figure 3-14, Figure 3-15, and Figure 3-16. Added information to Chapter 4, Mechanical Drawings, Chapter 5, Thermal Specifications, and Chapter 6, Package Marking.
06/14/11	1.2	Added Virtex-7 device information including updating Table 1-1, adding Table 1-5, Table 1-8, Table 2-3, and Table 3-3. In Table 1-9, updated Note 3, the Configuration Pins section, and the Analog to Digital Converter (XADC) Pins section. Updated Figure 3-11, Figure 3-12, Figure 3-15, Figure 3-16, Figure 3-19, Figure 3-20, Figure 3-23, Figure 3-24, Figure 3-27, Figure 3-28, Figure 3-31, and Figure 3-32. Added Figure 3-33 through Figure 3-88. Added Figure 4-7 the mechanical drawing for the Kintex-7 devices FFG1156 package. Also added some Virtex-7 device mechanical drawings in Figure 4-8 through Figure 4-11. Added thermal resistance data to Table 5-1.
10/03/11	1.3	Added Artix-7 device information including updating Table 1-1, adding Table 1-3, Table 1-6, Table 2-1, and Table 3-1. Clarified the interposer in Figure 1-12 and Figure 1-13. Revised horizontal center for the XC7VX415T in Figure 1-15. Updated the DXP_0/DXN_0 description and notes in Table 1-9. Added devices to the Die Level Bank Numbering Overview section. Clarified the I/O banks summary: section. Added Artix-7 device diagrams in the CSG324 package: Figure 3-1 through Figure 3-8. Added XC7V585T device diagrams Figure 3-53 through Figure 3-60. Moved AD4P/N, AD12P/N, and AD5P/N pins from [IO_L2P_T0_35:IO_L4N_T0_35] to [IO_L1P_T0_35:IO_L3N_T0_35] in Figure 3-61, Figure 3-65, Figure 3-69, Figure 3-73, Figure 3-77, Figure 3-81, and Figure 3-85. Fixed the labeling for EMCCLK in Figure 3-37, Figure 3-41, Figure 3-45, Figure 3-49, Figure 3-53, Figure 3-61, Figure 3-65, Figure 3-69, Figure 3-73, Figure 3-77, Figure 3-81, and Figure 3-85. Updated the mechanical drawings for Figure 4-9 and Figure 4-11. Updated thermal resistance data in Table 5-1. Updated Chapter 6, Package Marking.
10/17/11	1.4	Revised the FBG484 Package section describing XC7K160T Banks. Added the mechanical drawings: Figure 4-10 and Figure 4-12. Updated Figure 4-11 to include the FF(G)1928 package. Added thermal resistance data to Table 5-1.

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About This Guide

Xilinx® 7 series FPGAs include three unified FPGA families that are all designed for lowest power to enable a common design to scale across families for optimal power, performance, and cost. The Artix™-7 family is optimized for lowest cost and absolute power for the highest volume applications. The Virtex®-7 family is optimized for highest system performance and capacity. The Kintex™-7 family is an innovative class of FPGAs optimized for the best price-performance. This guide serves as a technical reference describing the 7 series packaging and pinout specifications.

This 7 series packaging and pinout specification, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/7.

Guide Contents

This manual contains the following chapters:

- Chapter 1, Packaging Overview
- Chapter 2, 7 Series FPGAs Package Files
- Chapter 3, Device Diagrams
- Chapter 4, Mechanical Drawings
- Chapter 5, Thermal Specifications
- Chapter 6, Package Marking
- Appendix A, Recommended PCB Design Rules for BGA Packages

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Chapter 1

Packaging Overview

Summary

This chapter covers the following topics:

- Introduction
- Device/Package Combinations and Maximum I/Os
- Pin Definitions
- Die Level Bank Numbering Overview

Introduction

This section describes the pinouts for the 7 series FPGAs in 0.5 mm chip-scale, 0.8 mm chip scale, and 1.0 mm in various fine pitch and flip-chip BGA packages.

Artix™-7 and Kintex™-7 devices are offered in low-cost, space-saving packages that are optimally designed for the maximum number of user I/Os.

Virtex®-7 and Virtex-7X devices are offered exclusively in high performance flip-chip BGA packages that are optimally designed for improved signal integrity and jitter.

Package inductance is minimized as a result of optimal placement and even distribution as well as an increased number of Power and GND pins.

All packages are available as Pb-free (G) with selected packages including a Pb-only option.

All of the 7 series devices supported in a particular package are pinout compatible and are listed in the same table (one table per package). Pins that are not available for the smaller devices are listed as "No Connects".

Each device is split into I/O banks to allow for flexibility in the choice of I/O standards (see UG471, *7 Series FPGAs SelectIO Resources User Guide*). Global pins, including JTAG, configuration, and power/ground pins, are listed at the end of each table. Table 1-9 provides definitions for all pin types.

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Device/Package Combinations and Maximum I/Os

Table 1-1 shows the maximum number of user I/Os possible in the 7 series FPGAs BGA packages. Some devices are available in both Pb and Pb-free (additional G) packages as standard ordering options.

Table 1-1: **7 Series FPGAs Package Specifications**

Packages[1]	Description	Package Specifications			
		Package Type	Pitch (mm)	Size (mm)	Maximum I/Os[2]
CPG236	Wire-bond chip-scale	BGA	0.5	10 x 10	140
CSG225		BGA	0.8	12 x 12	100
CSG324		BGA	0.8	15 x 15	210
FTG256	Wire-bond fine-pitch	BGA	1.0	17 x 17	170
FGG484		BGA	1.0	23 x 23	285
FGG676		BGA	1.0	27 x 27	300
FB(G)484	Flip-chip bare-die	BGA	1.0	23 x 23	285
FB(G)676		BGA	1.0	27 x 27	400
FB(G)900		BGA	1.0	31 x 31	500
FF(G)676	Flip-chip fine-pitch	BGA	1.0	27 x 27	400
FF(G)900		BGA	1.0	31 x 31	500
FF(G)901		BGA	1.0	31 x 31	380
FF(G)1156		BGA	1.0	35 x 35	600
FF(G)1157		BGA	1.0	35 x 35	600
FF(G)1158		BGA	1.0	35 x 35	350
FF(G)1761		BGA	1.0	42.5 x 42.5	850
FF(G)1926		BGA	1.0	45 x 45	720
FF(G)1927		BGA	1.0	45 x 45	600
FF(G)1928		BGA	1.0	45 x 45	480
FF(G)1930		BGA	1.0	45 x 45	1000
FL(G)1761		BGA	1.0	42.5 x 42.5	850
FL(G)1925		BGA	1.0	45 x 45	1200
FL(G)1928		BGA	1.0	45 x 45	480
FL(G)1930		BGA	1.0	45 x 45	1100
FH(G)1761		BGA	1.0	45 x 45	850

Notes:

1. Leaded package options (FFxxx/FBxxx) are available for the Kintex-7 XC7K160T, XC7K325T, XC7K355T, XC7K410T, XC7K420T, and XC7K480Tdevices.
2. The maximum I/O numbers do not include pins in the configuration Bank 0 (Table 1-2) or the GTX serial transceivers.

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Table 1-2 lists the 21 dedicated I/O pins.

Table 1-2: **7 series FPGAs I/O Pins in the Dedicated Configuration Bank (Bank0)**

DXP_0	VCCBATT_0	INIT_B_0	M0_0	TDO_0	TDI_0	GNDADC_0
DXN_0	DONE_0	VN_0	M1_0	TCK_0	VREFN_0	VCCADC_0
PROGRAM_B_0	CCLK_0	VP_0	M2_0	TMS_0	VREFP_0	CFGBVS_0

Serial Transceiver Channels by Device/Package

Table 1-3 lists the quantity of GTP serial transceiver channels for the Artix-7 FPGAs. Table 1-4 lists the quantity of GTX serial transceiver channels for the Kintex-7 FPGAs. Table 1-5 lists the quantity of GTX and GTH serial transceiver channels for the Virtex-7 FPGAs. In all devices, a serial transceiver channel is one set of MGTRXP, MGTRXN, MGTTXP, and MGTTXN pins.

Table 1-3: **Serial Transceiver Channels (GTPs) by Device/Package (Artix-7 FPGAs)**

Device	GTP Channels by Package								
	CPG236	CSG225	CSG324	FTG256	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A8	0	0	0	–	–	–	–	–	–
XC7A15	0	0	0	–	–	–	–	–	–
XC7A30T	–	4	0	0	4	–	–	–	–
XC7A50T	–	4	0	0	4	–	–	–	–
XC7A100T	–	–	0	0	4	8	–	–	–
XC7A200T	–	–	–	–	–	–	4	8	16
XC7A350T	–	–	–	–	–	–	4	8	16

Table 1-4: **Serial Transceiver Channels (GTXs) by Device/Package (Kintex-7 FPGAs)**

Device	GTX Channels by Package						
	FBG484	FBG676	FBG900	FFG676	FFG900	FFG901	FFG1156
XC7K70T	4	8	–	–	–	–	–
XC7K160T	4	8	–	8	–	–	–
XC7K325T	–	8	16	8	16	–	–
XC7K355T	–	–	–	–	–	24	–
XC7K410T	–	8	16	8	16	–	–
XC7K420T	–	–	–	–	–	28	28
XC7K480T	–	–	–	–	–	28	32

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Table 1-5: **Serial Transceiver Channels (GTX/GTH) by Device/Package (Virtex-7 FPGAs)**

Device	GTX or GTH Channels by Package											
	FFG 1157	FFG 1158	FFG 1761	FFG 1926	FFG 1927	FFG 1928	FFG 1930	FLG 1761	FLG 1925	FLG 1928	FLG 1930s	FHG 1761
XC7V585T	20 0	–	36 0	–	–	–	–	–	–	–	–	– –
XC7V1500T	–	–	–	–	–	–	–	36 0	–	–	–	– –
XC7V2000T	–	–	–	–	–	–	–	–	16 0	–	–	36 0
XC7VX330T	0 20	–	0 28	–	–	–	–	–	–	–	–	–
XC7VX415T	0 20	0 48	–	–	0 48	–	–	–	–	–	–	–
XC7VX485T	20 0	48 0	28 0	–	56 0	–	24 0	–	–	–	–	–
XC7VX550T	–	0 48	–	–	0 64	–	–	–	–	–	–	–
XC7VX690T	0 20	0 48	0 36	0 64	0 80	–	0 24	–	–	–	–	–
XC7VX980T	–	–	–	0 64	–	0 72	0 24	–	–	–	–	–
XC7VX1140T	–	–	–	–	–	–	–	–	–	0 96	0 24	–

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Table 1-6 shows the number of available I/Os and the number of differential I/Os for each Artix-7 device/package combination. Table 1-7 shows the number of available I/Os and the number of differential I/Os for each Kintex-7 device/package combination. Table 1-8 shows the number of available I/Os and the number of differential I/Os for each Virtex-7 device/package combination. When applicable, it also lists the number of user I/Os in the 3.3V-capable high-range (HR) banks and the number of 1.8V-capable high-performance (HP) banks.

Table 1-6: **Available I/O Pin/Device/Package Combinations for Artix-7 FPGAs**

Artix-7 Devices	User I/O Pins	Artix-7 Packages: HR I/O Banks Only								
		CPG236	CSG225	CSG324	FTG256	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A8	User I/O	140	–	200	170	–	–	–	–	–
	Differential		–	192		–	–	–	–	–
XC7A15	User I/O	140	–	200	170	–	–	–	–	–
	Differential		–	192		–	–	–	–	–
XC7A30T	User I/O	–	100	210	170	250	–	–	–	–
	Differential	–		202			–	–	–	–
XC7A50T	User I/O	–	100	210	170	250	–	–	–	–
	Differential	–		202			–	–	–	–
XC7A100T	User I/O	–	–	210	170	285	300	–	–	–
	Differential	–	–	202				–	–	–
XC7A200T	User I/O	–	–	–	–	–	–	285	400	500
	Differential	–	–	–	–	–	–			
XC7A350T	User I/O	–	–	–	–	–	–	285	400	600
	Differential	–	–	–	–	–	–			

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Table 1-7: **Available I/O Pin/Device/Package Combinations for Kintex-7 FPGAs**

Kintex-7 Devices	User I/O Pins	Kintex-7 Packages: HR and HP I/O Banks													
		FBG484		FBG676		FBG900		FFG676		FFG900		FFG901		FFG1156	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7K70T	User I/O	100	185	100	200	–	–	–	–	–	–	–	–	–	–
	Differential	96	179	96	192	–	–	–	–	–	–	–	–	–	–
XC7K160T	User I/O	100	185	150	250	–	–	150	250	–	–	–	–	–	–
	Differential	96	179	144	240	–	–	144	240	–	–	–	–	–	–
XC7K325T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–
XC7K355T	User I/O	–	–	–	–	–	–	–	–	–	–	0	300	–	–
	Differential	–	–	–	–	–	–	–	–	–	–	0	288	–	–
XC7K410T	User I/O	–	–	150	250	150	350	150	250	150	350	–	–	–	–
	Differential	–	–	144	240	144	336	144	240	144	336	–	–	–	–
XC7K420T	User I/O	–	–	–	–	–	–	–	–	–	–	0	350	0	350
	Differential	–	–	–	–	–	–	–	–	–	–	0	336	0	366
XC7K480T	User I/O	–	–	–	–	–	–	–	–	–	–	0	380	0	400
	Differential	–	–	–	–	–	–	–	–	–	–	0	366	0	384

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Table 1-8: **Available I/O Pin/Device/Package Combinations for Virtex-7 FPGAs**

Virtex-7 Devices	User I/O Pins	Virtex-7 Packages: HR and HP I/O Banks																					
		FFG		FFG		FFG		FFG		FFG		FFG		FFG		FLG		FLG		FLG		FLG		FHG	
		1157		1158		1761		1926		1927		1928		1930		1761		1925		1928		1930		1761	
		HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR	HP	HR
XC7V 585T	User	600	0	–		750	100	–		–		–		–		–		–		–		–		–	
	Diff	576	0	–		720	96	–		–		–		–		–		–		–		–		–	
XC7V 1500T	User	–		–		–		–		–		–		–		850	0	–		–		–		–	
	Diff	–		–		–		–		–		–		–		816	0	–		–		–		–	
XC7V 2000T	User	–		–		–		–		–		–		–		–		1200	0	–		–		850	0
	Diff	–		–		–		–		–		–		–		–		1152	0	–		–		816	0
XC7VX 330T	User	600	0	–		650	50	–		–		–		–		–		–		–		–		–	
	Diff	576	0	–		624	48	–		–		–		–		–		–		–		–		–	
XC7VX 415T	User	600	0	350	0	–		–		600	0	–		–		–		–		–		–		–	
	Diff	576	0	336	0	–		–		576	0	–		–		–		–		–		–		–	
XC7VX 485T	User	600	0	350	0	700	0	–		600	0	–		700	0	–		–		–		–		–	
	Diff	576	0	336	0	672	0	–		576	0	–		672	0	–		–		–		–		–	
XC7VX 550T	User	–		350	0	–		–		600	0	–		–		–		–		–		–		–	
	Diff	–		336	0	–		–		576	0	–		–		–		–		–		–		–	
XC7VX 690T	User	600	0	350	0	850	0	720	0	600	0	–		1000	0	–		–		–		–		–	
	Diff	576	0	336	0	816	0	690	0	576	0	–		960	0	–		–		–		–		–	
XC7VX 980T	User	–		–		–		720	0	–		480	0	900	0	–		–		–		–		–	
	Diff	–		–		–		690	0	–		460	0	864	0	–		–		–		–		–	
XC7VX 1140T	User	–		–		–		–		–		–		–		–		–		480	0	1100	0	–	
	Diff	–		–		–		–		–		–		–		–		–		460	0	1056	0	–	

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Pin Definitions

Table 1-9 lists the pin definitions used in 7 series FPGAs packages.

Note: There are dedicated general purpose user I/O pins listed separately in Table 1-9. There are also multi-function pins where the pin names start with either IO_LXXY_ZZZ_# or IO_XX_ZZZ_#, where ZZZ represents one or more functions in addition to being general purpose user I/O. If not used for their special function, these pins can be user I/O.

Table 1-9: **7 series FPGAs Pin Definitions**

Pin Name	Type	Direction	Description
User I/O Pins			
IO_LXXY_# IO_XX_#	Dedicated	Input/ Output	Most user I/O pins are capable of differential signaling and can be implemented as pairs. The top and bottom I/O pins are always single ended. Each user I/O is labeled IO_LXXY_#, where: • IO indicates a user I/O pin. • L indicates a differential pair, with XX a unique pair in the bank and Y = [P | N] for the positive/negative sides of the differential pair. • # indicates a bank number.
Configuration Pins			
For more information, see the *Configuration Pin Definitions* table in UG470, *7 Series FPGAs Configuration User Guide*.			
CCLK_0	Dedicated(1)	Input/ Output	Configuration clock. Output in Master mode or input in Slave mode.
DONE_0	Dedicated(1)	Bidirectional	Active High, DONE indicates successful completion of configuration.
INIT_B_0	Dedicated(1)	Bidirectional (open-drain)	Active Low, indicates initialization of configuration memory.
M0_0, M1_0, or M2_0	Dedicated(1)	Input	Configuration mode selection
PROGRAM_B_0	Dedicated(1)	Input	Active Low, asynchronous reset to configuration logic.
TCK_0	Dedicated(1)	Input	JTAG clock.
TDI_0	Dedicated(1)	Input	JTAG data input.
TDO_0	Dedicated(1)	Output	JTAG data output.
TMS_0	Dedicated(1)	Input	JTAG mode select.
CFGBVS_0	Dedicated(1)	Input	This pin selects the preconfiguration I/O standard type for the dedicated and multi-function configuration banks 0, 14, and 15. If the V_{CCO} for banks 0, 14, or 15 is 2.5V or 3.3V, then this pin must be connect to V_{CCO_0}. If the V_{CCO} for banks 0, 14, and 15 are less than or equal to 1.8V, then this pin should be connected to GND. ***Note:*** To avoid device damage, this pin must be connected correctly. See the *Configuration Bank Voltage Select* section in UG470: *7 Series FPGAs Configuration User Guide* for more information.
D00 through D31	Multi-function	Bidirectional	Configuration data pins.

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Table 1-9: **7 series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
ADV_B	Multi-function	Output	BPI Flash address valid output
A00 through A28	Multi-function	Output	Address A00–A28 BPI address output.
RS0 or RS1	Multi-function	Output	RS0 and RS1 revision select output.
FCS_B	Multi-function	Output	BPI and SPI flash chip select.
FOE_B	Multi-function	Output	BPI flash output enable.
MOSI	Multi-function	Output	SPI flash command output. Also known as the SPI bus master output, slave input signal.
FWE_B	Multi-function	Output	BPI flash write enable.
DOUT	Multi-function	Output	Data output for serial daisy-chain configuration.
CSO_B	Multi-function	Output	Active Low chip-select output for parallel daisy-chain.
CSI_B	Multi-function	Input	SelectMAP active Low chip-select input.
PUDC_B	Multi-function	Input	Active Low input enables internal pull-ups during configuration on all SelectIO pins: 0 = Weak preconfiguration I/O pull-up resistors enabled 1 = Weak preconfiguration I/O pull-up resistors disabled
RDWR_B	Multi-function	Input	SelectMAP data bus direction control signal for reading or writing configuration data.
EMCCLK	Multi-function	Input	External master configuration clock.
Power/Ground Pins			
GND	Dedicated	N/A	Ground.
VCCAUX	Dedicated	N/A	1.8V power-supply pins for auxiliary circuits.
VCCAUX_IO_G#(2)	Dedicated	N/A	1.8V/2.0V power-supply pins for auxiliary I/O circuits.
VCCINT	Dedicated	N/A	0.9V/1.0V power-supply pins for the internal core logic.
VCCO_#(3)	Dedicated	N/A	Power-supply pins for the output drivers (per bank).
VCCBRAM	Dedicated	N/A	1.0V power-supply pins for the FPGA logic block RAM.
VCCBATT_0	Dedicated	N/A	Decryptor key memory backup supply; this pin should be tied to the appropriate V_{CC} or GND when not used.(4)
VREF	Multi-function	N/A	These are input threshold voltage pins. They become user I/Os when an external threshold voltage is not needed (per bank).
Analog to Digital Converter (XADC) Pins			
For more information, see the *XADC Package Pins* table in UG480, *7 Series FPGAs XADC User Guide*.			
VCCADC_0(5)	Dedicated	N/A	XADC analog positive supply voltage.
GNDADC_0(5)	Dedicated	N/A	XADC analog ground reference.
VP_0(5)	Dedicated	Input	XADC dedicated differential analog input (positive side).
VN_0(5)	Dedicated	Input	XADC dedicated differential analog input (negative side).

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Table 1-9: **7 series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
VREFP_0[5]	Dedicated	N/A	1.25V reference input.
VREFN_ 0[5]	Dedicated	N/A	1.25V reference GND reference.
AD0P through AD15P AD0N through AD15N	Multi-function	Input	XADC (analog-to-digital converter) differential auxiliary analog inputs 0–15. Auxiliary channels 6, 7, 13, 14, and 15 are not supported on Kintex-7 devices.
Multi-gigabit Serial Transceiver Pins (GTXE2 and GTHE2)			
For more information on the GTXE2 pins see the *Pin Description and Design Guidelines* section in UG476, *7 Series FPGAs GTX Transceivers User Guide*.			
MGTXRXP[0:3]	Dedicated	Input	Positive differential receive port GTX Quad.
MGTXRXN[0:3]	Dedicated	Input	Negative differential receive port GTX Quad.
MGTXTXP[0:3]	Dedicated	Output	Positive differential transmit port GTX Quad.
MGTXTXN[0:3]	Dedicated	Output	Negative differential transmit port GTX Quad.
MGTHRXP[0:3]	Dedicated	Input	Positive differential receive port GTH Quad.
MGTHRXN[0:3]	Dedicated	Input	Negative differential receive port GTH Quad.
MGTHTXP[0:3]	Dedicated	Output	Positive differential transmit port GTH Quad.
MGTHTXN[0:3]	Dedicated	Output	Negative differential transmit port GTH Quad.
MGTAVCC_G#	Dedicated	Input	1.0V analog power-supply pin for the receiver and transmitter internal circuits.
MGTAVTT_G#	Dedicated	Input	1.2V analog power-supply pin for the transmit driver.
MGTVCCAUX_G#	Dedicated	Input	1.8V auxiliary analog Quad PLL (QPLL) voltage supply for the transceivers.
MGTREFCLK0/1P	Dedicated	Input	Positive differential reference clock for the transceivers.
MGTREFCLK0/1N	Dedicated	Input	Negative differential reference clock for the transceivers.
MGTAVTTRCAL	Dedicated	N/A	Precision reference resistor pin for internal calibration termination. Not used for Artix-7 devices.
MGTRREF	Dedicated	Input	Precision reference resistor pin for internal calibration termination.
Other Pins			
RSVD	Dedicated	N/A	Reserved. No Connection; leave floating.
MRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, BUFGs, and MMCMs/PLLs. In addition, these pins can drive the BUFMR for multi-region BUFIO and BUFR support. These pins become regular user I/Os when not needed as a clock. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The MRCC (multi-region) pins, when used as single region resource, can drive four BUFIOs and four BUFR in a single bank.

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Table 1-9: **7 series FPGAs Pin Definitions *(Cont'd)***

Pin Name	Type	Direction	Description
SRCC	Multi-function	Input	These are the clock capable I/Os driving BUFRs, BUFIOs, and MMCMs/PLLs. These pins become regular user I/Os when not needed for clocks. When connecting a single-ended clock to the differential CC pair of pins, it must be connected to the positive (P) side of the pair. The SRCC (single region) pins can drive four BUFIOs and four BUFRs in a single bank.
VRN(6)	Multi-function	N/A	This pin is for the DCI voltage reference resistor of N transistor (per bank, to be pulled High with reference resistor).
VRP(6)	Multi-function	N/A	This pin is for the DCI voltage reference resistor of P transistor (per bank, to be pulled Low with reference resistor).
DXP_0, DXN_0	Dedicated	Input	Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND. To use the thermal diode an appropriate external thermal monitoring IC must be added. Consult the external thermal monitoring IC data sheet for usage guidelines. The recommended temperature monitoring solution for 7 series FPGAs uses the temperature sensor in the XADC block.
T0, T1, T2, or T3	Multi-function	Input	This pin belongs to the memory byte group 0-3.
T0_DQS, T1_DQS, T2_DQS, or T3_DQS	Multi-function	Input	The DDR DQS strobe pin that belongs to the memory byte group T0–T3.

Notes:

1. All dedicated pins (JTAG and configuration) are powered by V_{CCO_0}.
2. For devices that do not include VCCAUX_IO_G# pins, auxiliary I/O circuits are powered by VCCAUX pins.
3. V_{CCO} pins in unbonded banks must be connected to the V_{CCO} for that bank for package migration. Do NOT connect unbonded V_{CCO} pins to different supplies. Without a package migration requirement, V_{CCO} pins in unbonded banks can be tied to a common supply (V_{CCO} or ground).
4. Refer to the data sheet for V_{CCBATT_0} specifications.
5. See UG480, *7 Series FPGAs XADC User Guide* for the default connections required to support on-chip monitoring.
6. The DCI guidelines in the 7 series FPGAs are different from previous Virtex device DCI guidelines. See the DCI sections in UG471: *7 Series FPGAs SelectIO Resources User Guide* for more information on the VRN/VRP pins.

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Die Level Bank Numbering Overview

Banking and Clocking Summary

- The center clocking backbone contains all vertical clock tracks and clock buffer connectivity.
- The CMT backbone contains all vertical CMT connectivity and is located in the CMT column.
- Not all banks are bonded out in every part/package combination.
- GTP/GTX/GTH columns summary:
  - One bank = One GT Quad = Four transceivers = Four GTPE2s or GTXE2s or GTHE2 primitives.
  - Not all GT Quads are bonded out in every package.
- I/O banks summary:
  - Each bank has four pairs of clock capable (CC) inputs for four differential or four single ended clock inputs.
    - Can connect to the CMT in the same region and the region above and below (with restrictions).
    - Two MRCC pairs can connect to the BUFRs and BUFIOs in the same region/banks and the regions/banks above and below.
    - Two SRCCs pairs can only connect to the BUFRs and BUFIOs in the same region/bank.
    - There are no global clock pins (GC pins) in the 7 series FPGAs.
  - Each user I/O bank has 50 single-ended I/Os or 24 differential pairs (48 differential I/Os). The top and bottom I/O pin are always single ended. All 50 pads of a bank are not always bonded out to pins.
- Bank locations of dedicated and dual-purpose pins:
  - In most devices, banks 14 and 15 always contain the dual-purpose configuration pins. Bank 15 and 35 contains the XADC auxiliary inputs; however, in Kintex-7 devices, the auxiliary inputs are only in bank 15. Bank 0 contains the dedicated configuration pins.
  - In the XC7V1500T and XC7V2000T devices, banks 11 and 12 contain the dual-purpose configuration pins. Bank 12 and 32 contains the XADC auxiliary inputs. Bank 0 contains the dedicated configuration pins.
  - All dedicated configuration I/Os (bank 0) are 3.3V capable
- The physical XY locations for each IDELAYCTRL start at X0Y0 in the bottom left-most bank and are then increment by one starting with the lowest bank number in each column in the vertical Y direction and by one for each column in the horizontal X direction. IDELAYCTRLs are located in each of the HROWs.

Figure 1-1 through Figure 1-20 visually describe a die view of the FPGA bank numbering.

Note: The figures for some Artix-7 and Virtex-7 FPGAs are in development.

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XC7A8 or XC7A15 Banks

Figure 1-4 shows the I/O banks for the XC7A8 and XC7A15. These devices do not include transceiver banks.

CSG324 Package

- All HR banks are fully bonded out.

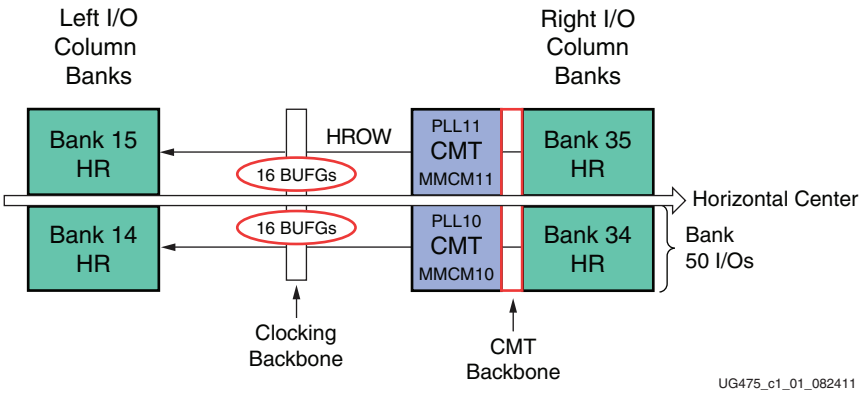

Figure 1-1: **XC7A8 and XC7A15 Banks**

XC7A30T or XC7A50T Banks

Figure 1-2 shows the I/O and transceiver banks for the XC7A30T or XC7A50T.

CSG324 Package

- HR bank 16 is partially bonded out.
- The GTX Quad bank 116 is not bonded out.

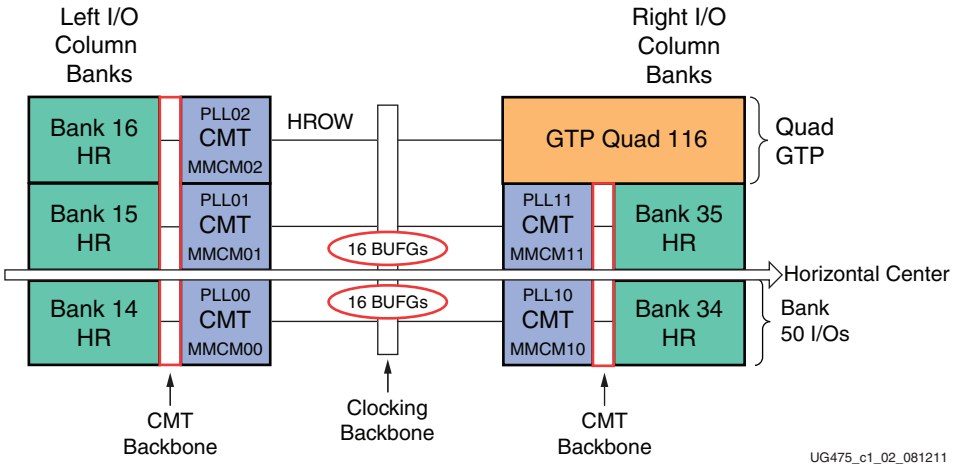

Figure 1-2: **XC7A30T and XC7A50T Banks**

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XC7A100T Bank

Figure 1-3 shows the I/O and transceiver banks for the XC7A100T.

CSG324 Package

- HR bank 13 is not bonded out.
- HR bank 16 is partially bonded out.
- The GTX Quad bank 116 is not bonded out.

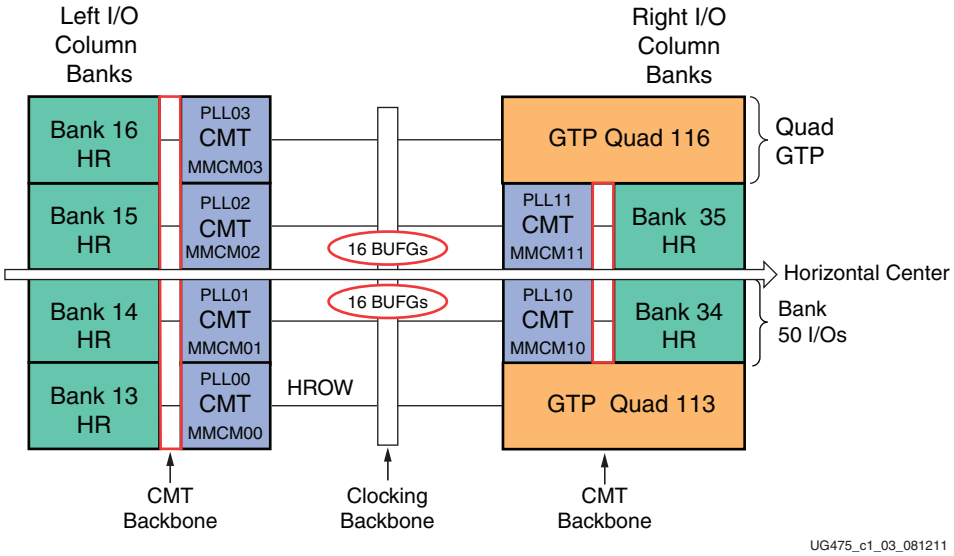

Figure 1-3: **XC7A100T Banks**

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XC7K70T Banks

Figure 1-4 shows the I/O and transceiver banks for the XC7K70T.

FBG484 Package

- HR bank 16 is partially bonded out.
- All HP banks are fully bonded out.
- The GTX Quad bank 116 is not bonded out.

FBG676 Package

- All HR and HP banks and the GTX Quads are fully bonded out in this package.

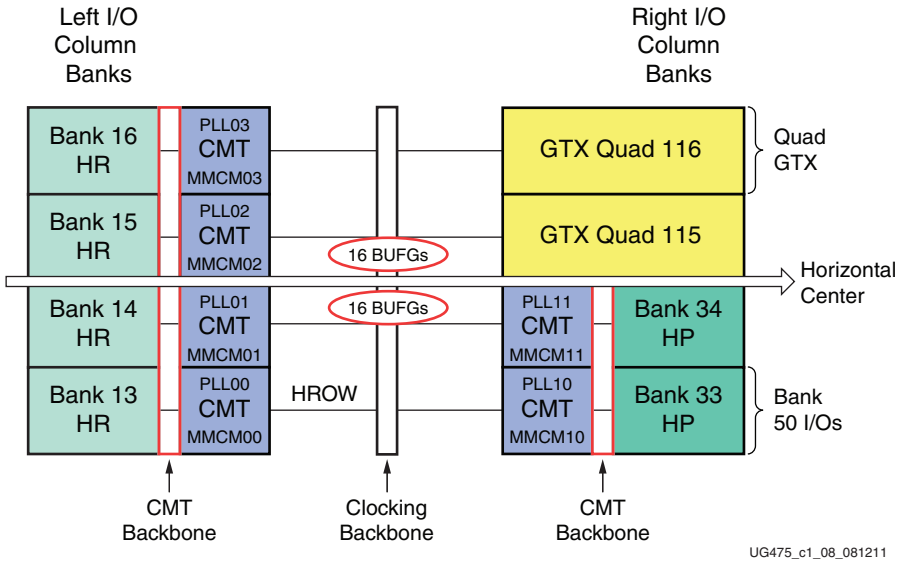

Figure 1-4: **XC7K70T Banks**

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XC7K160T Banks

Figure 1-5 shows the I/O and transceiver banks for the XC7K160T.

FBG484 Package

- HR bank 12 is not bonded out and bank 16 is partially bonded out.
- HP bank 32 is not bonded out.
- The GTX Quad bank 116 is not bonded out.

FBG676 and FFG676 Packages

- All HR and HP banks and the GTX Quads are fully bonded out in these packages.

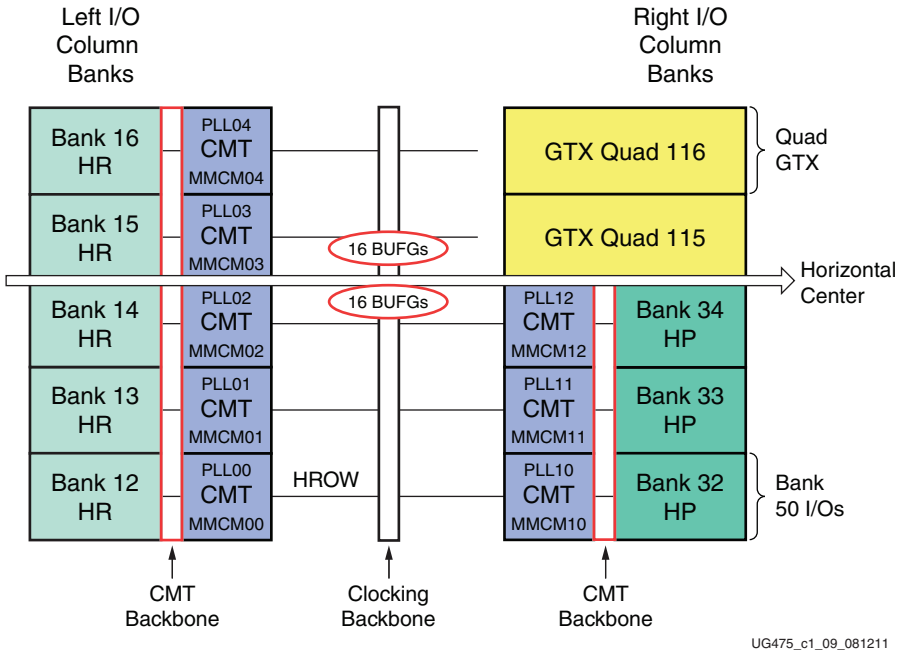

Figure 1-5: **XC7K160T Banks**

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XC7K325T Banks

Figure 1-6 shows the I/O and transceiver banks for the XC7K325T.

FBG676 and FFG676 Packages

- HR banks 17 and 18 are not bonded out.
- All HP banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900 and FFG900 Packages

All HR and HP banks and the GTX Quads are fully bonded out in these packages.

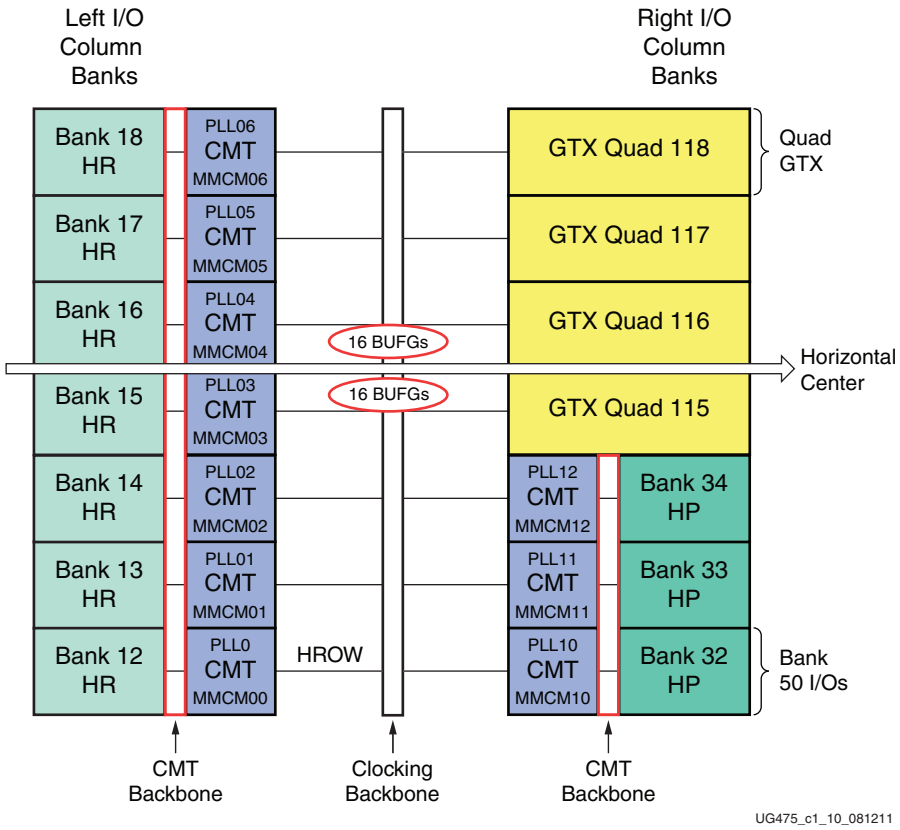

Figure 1-6: **XC7K325T Banks**

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XC7K355T Banks

Figure 1-7 shows the I/O and transceiver banks for the XC7K355T.

FFG901 Package

All HR banks and the GTX Quads are fully bonded out in this package.

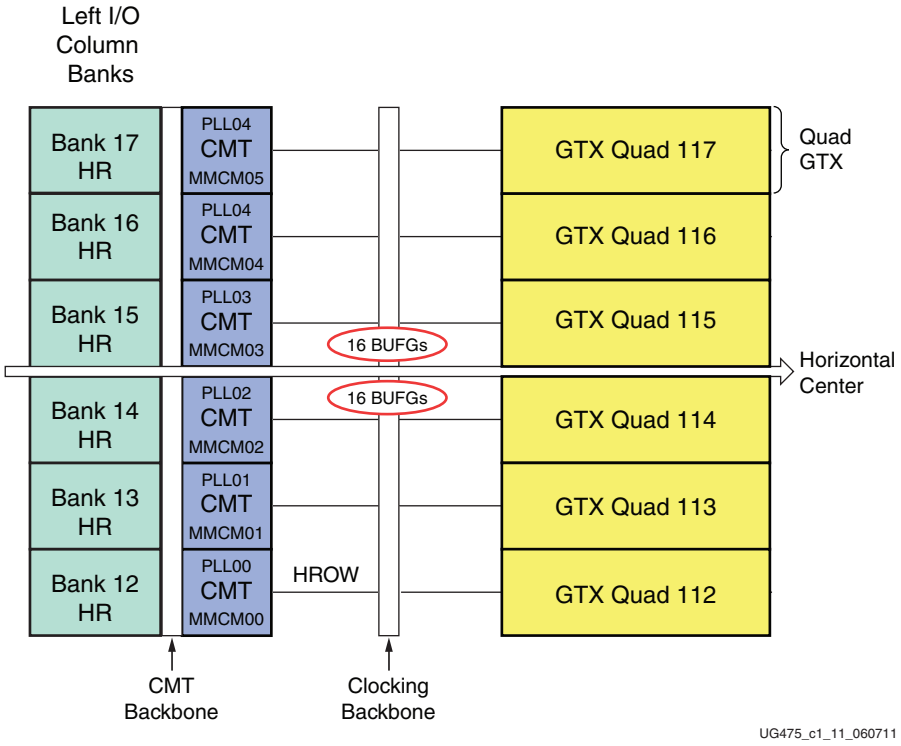

Figure 1-7: **XC7K355T Banks**

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XC7K410T Banks

Figure 1-8 shows the I/O and transceiver banks for the XC7K410T.

FBG676 and FFG676 Packages

- HR banks 17 and 18 are not bonded out.
- All HP banks are fully bonded out.
- GTX Quads 117 and 118 are not bonded out.

FBG900 and FFG900 Packages

All HR and HP banks and the GTX Quads are fully bonded out in these packages.

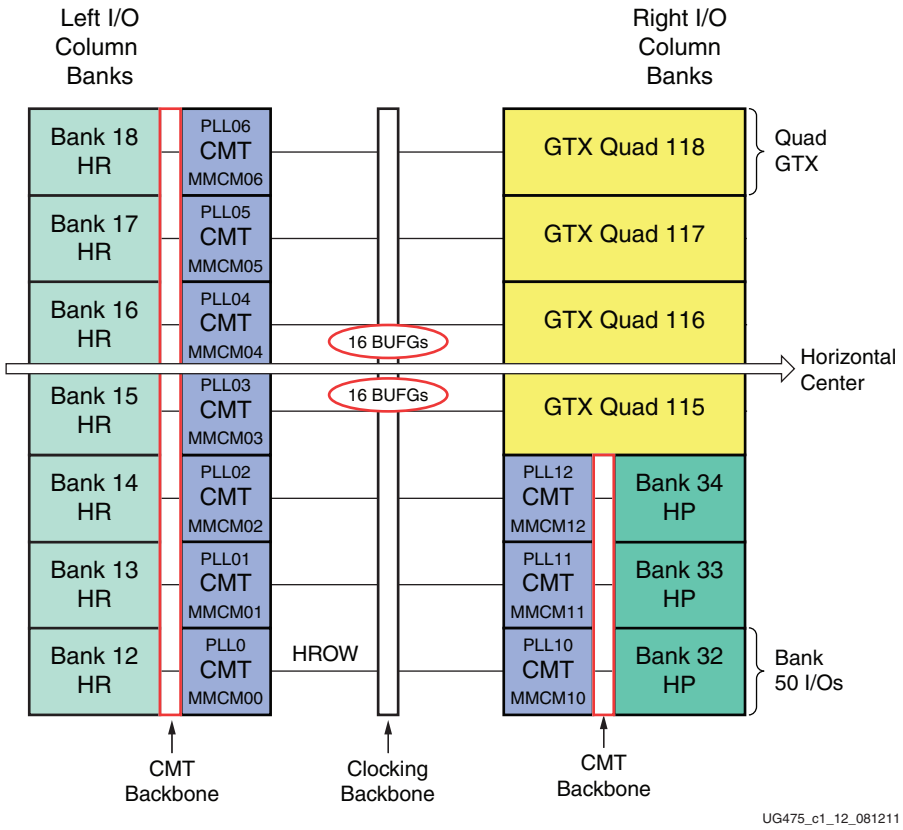

Figure 1-8: **XC7K410T Banks**

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XC7K420T Banks

Figure 1-9 shows the I/O and transceiver banks for the XC7K420T.

FFG901 and FFG1156 Packages

- All HR banks and the GTX Quads are fully bonded out in these packages.

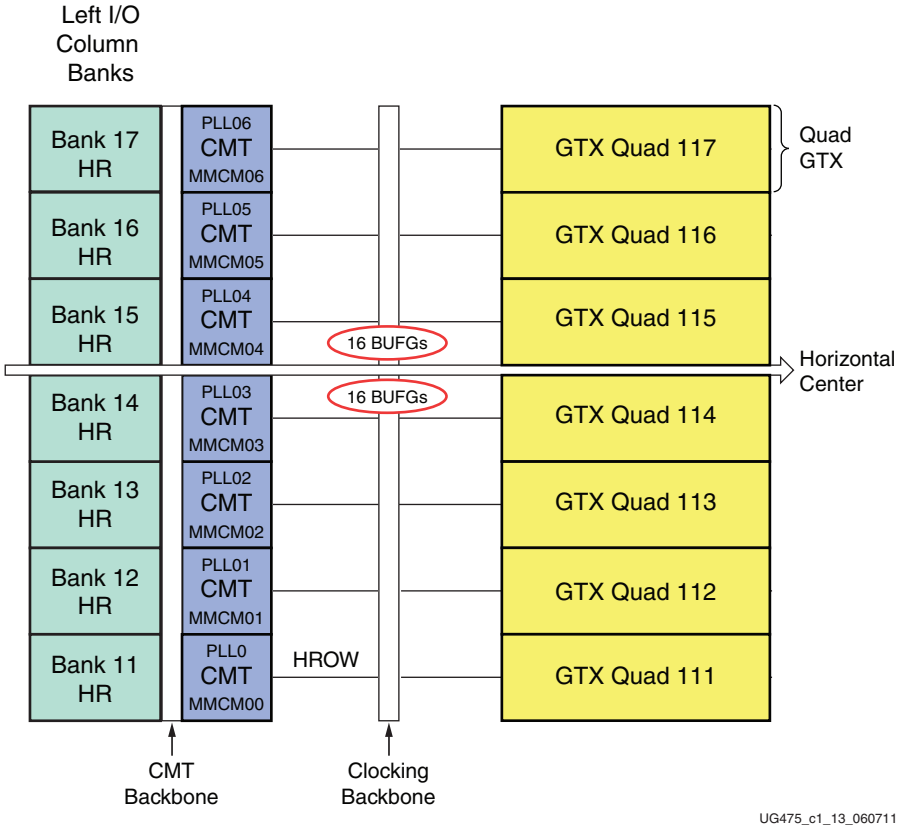

Figure 1-9: **XC7K420T Banks**

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XC7K480T Banks

Figure 1-10 shows the I/O and transceiver banks for the XC7K480T.

FFG901 Package

- HR bank 18 is not fully bonded out.
- GTX Quad bank 118 is not bonded out.

FFG1156 Package

All HR banks and the GTX Quads are fully bonded out in this package.

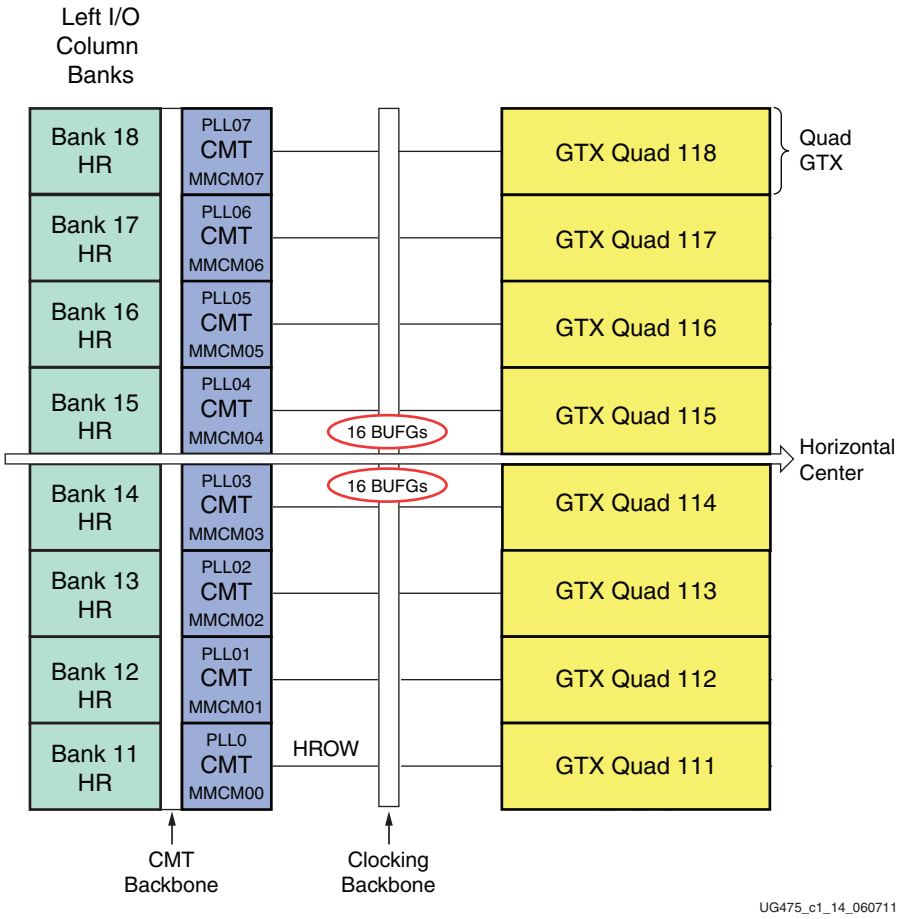

Figure 1-10: **XC7K480T Banks**

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XC7V585T Banks

Figure 1-11 shows the I/O and transceiver banks for the XC7V585T.

FFG1157 Package

- All HR banks (11, 12, and 13) are not bonded out.
- HP banks 31, 32, and 33 are not bonded out.
- GTX Quads 111, 112, 113, and 119 are not bonded out.

FFG1761 Package

- HR bank 11 is not bonded out.
- All HP banks and the GTX Quads are fully bonded out in this package.

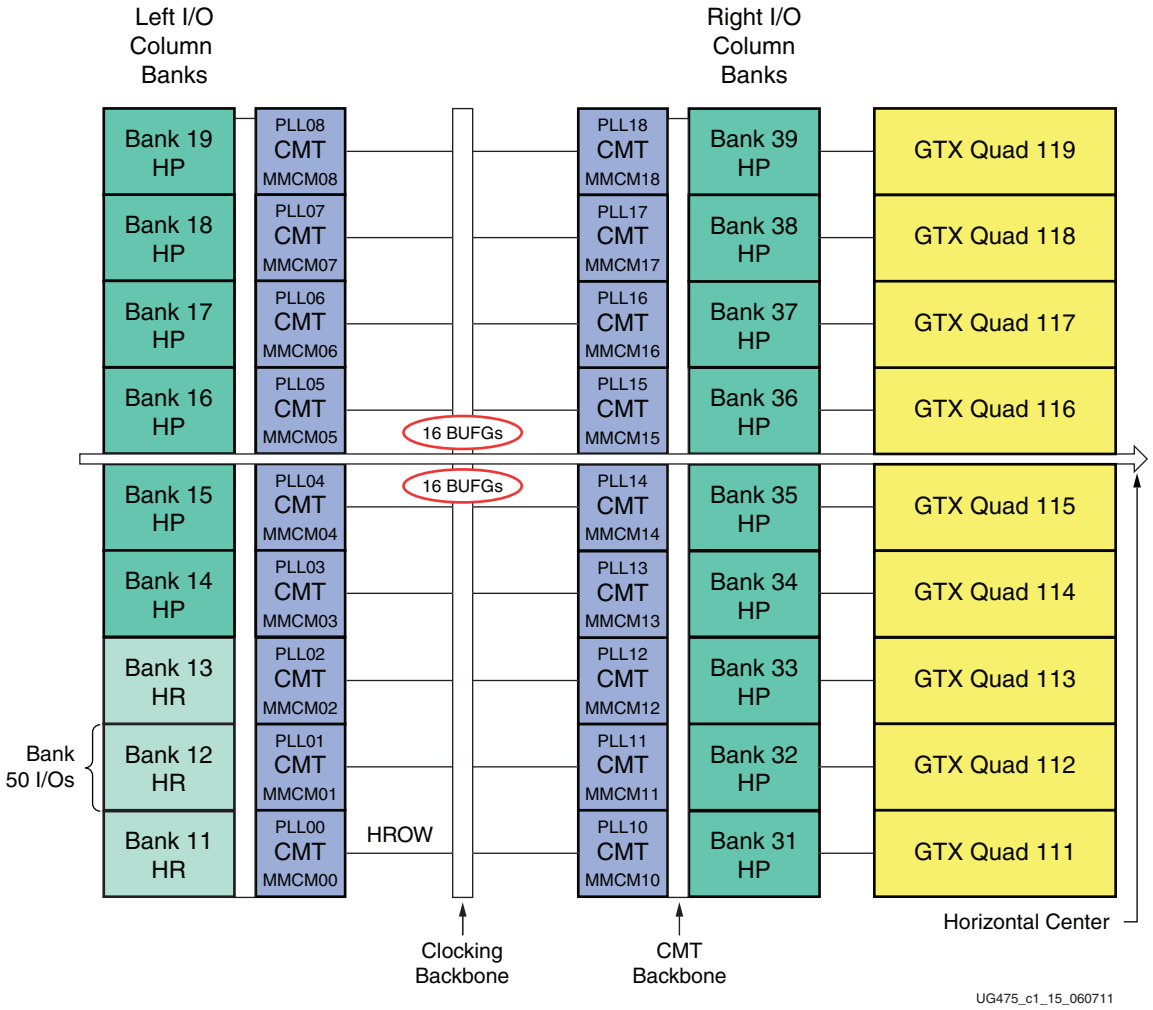

Figure 1-11: **XC7V585T Banks**

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XC7V1500T Banks

Figure 1-12 shows the I/O and transceiver banks for the XC7V1500T.

FLG1761 Package

- HP bank 11 is not bonded out.
- All the GTX Quads are fully bonded out in this package.

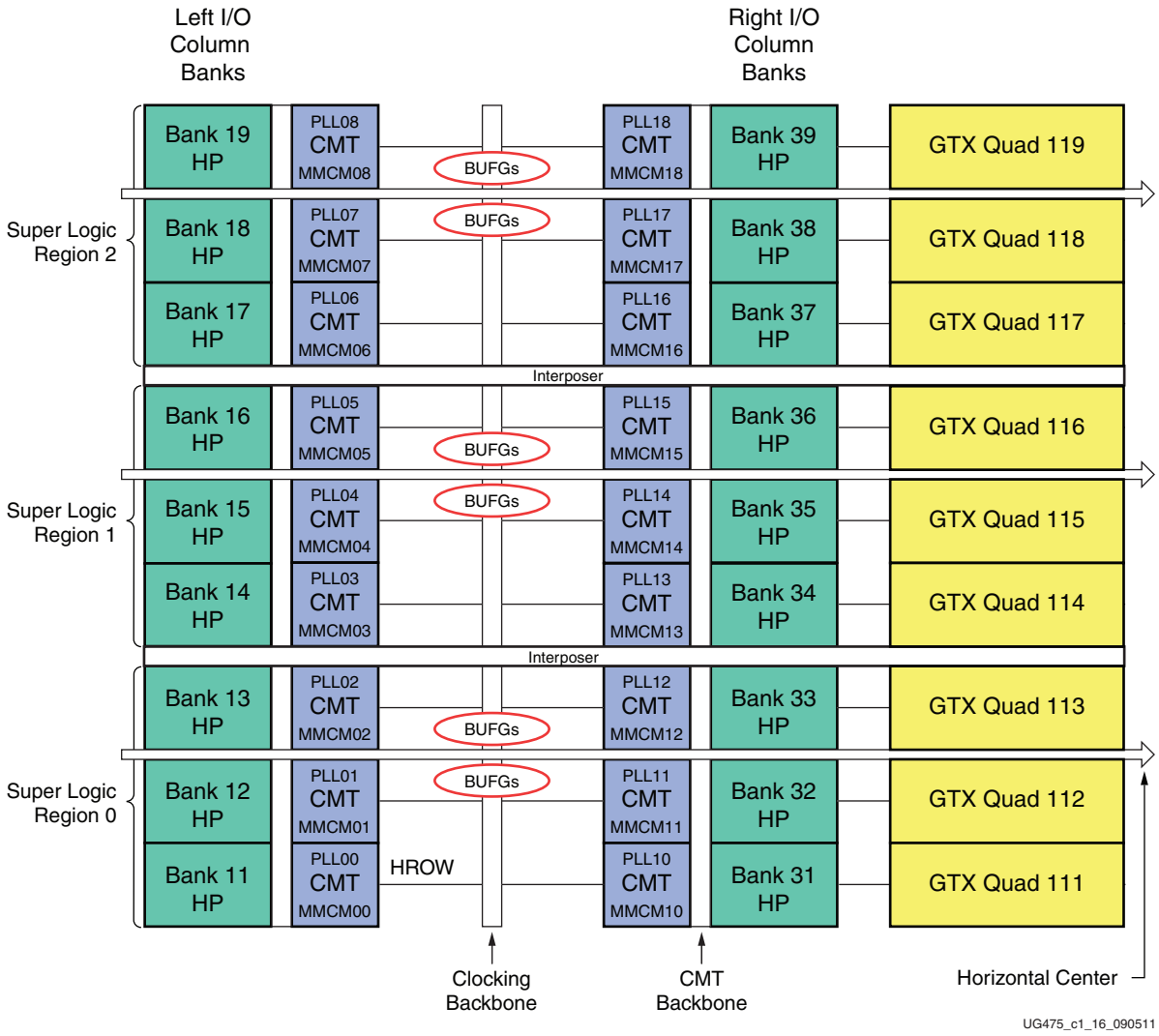

Figure 1-12: **XC7V1500T Banks**

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XC7V2000T Banks

Figure 1-13 shows the I/O and transceiver banks for the XC7V2000T.

FHG1761 Package

- HP banks 11, 20, 21, 22, 40, 41, and 42 are not bonded out.
- GTX Quads 120, 121, and 122 are not bonded out.

FLG1925 Package

- All HP banks are fully bonded out in this package.
- GTX Quads 111, 116, 117, 118, 119, 120, 121, and 122 are not bonded out.

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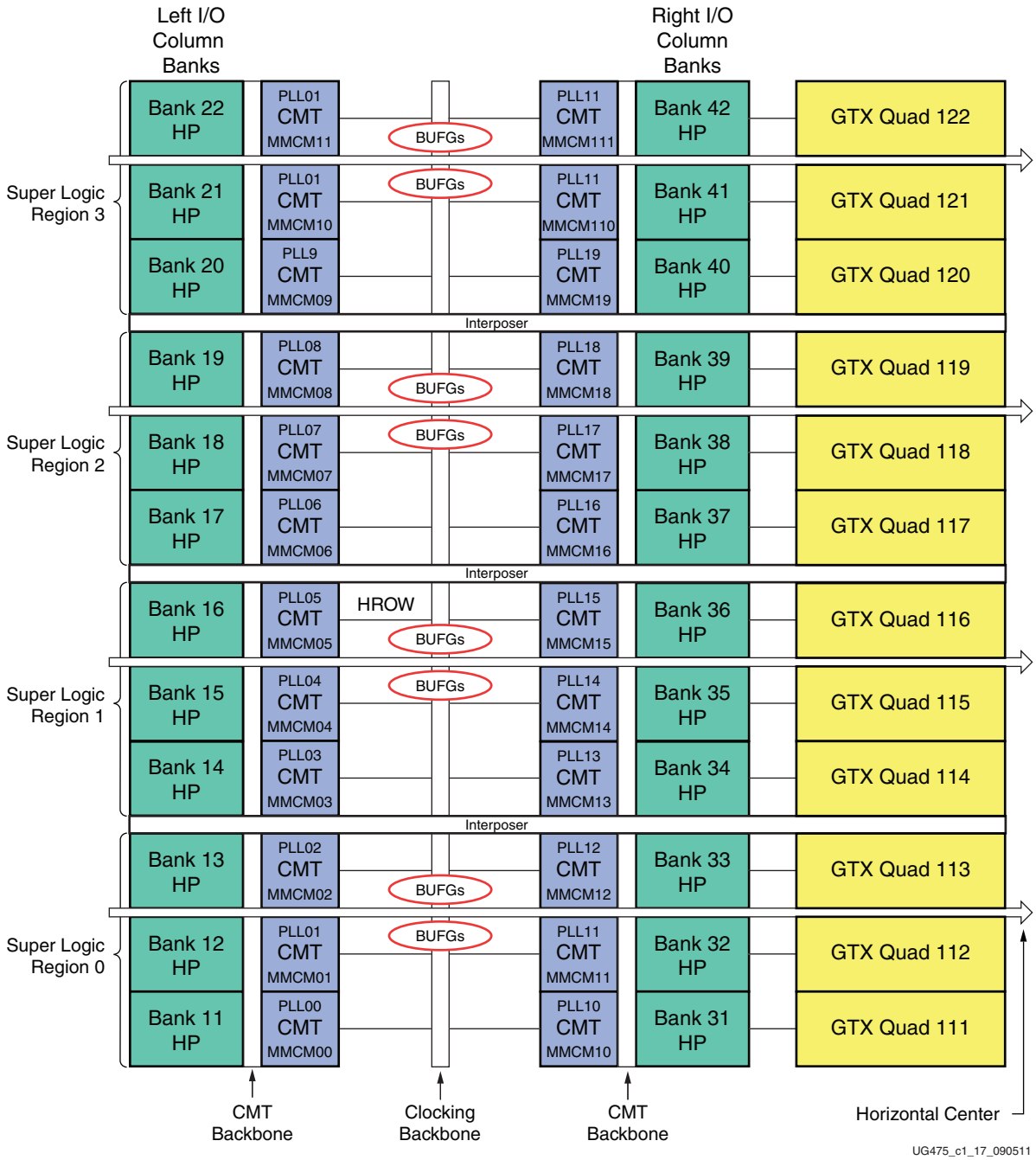

Figure 1-13: **XC7V2000T Banks**

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XC7VX330T Banks

Figure 1-14 shows the I/O and transceiver banks for the XC7VX330T.

FFG1157 Package

- HR bank 13 is not bonded out.
- HP bank 33 is not bonded out.
- GTH Quads 113 and 119 are not bonded out.

FFG1761 Package

All HR and HP banks and the GTH Quads are fully bonded out in this package.

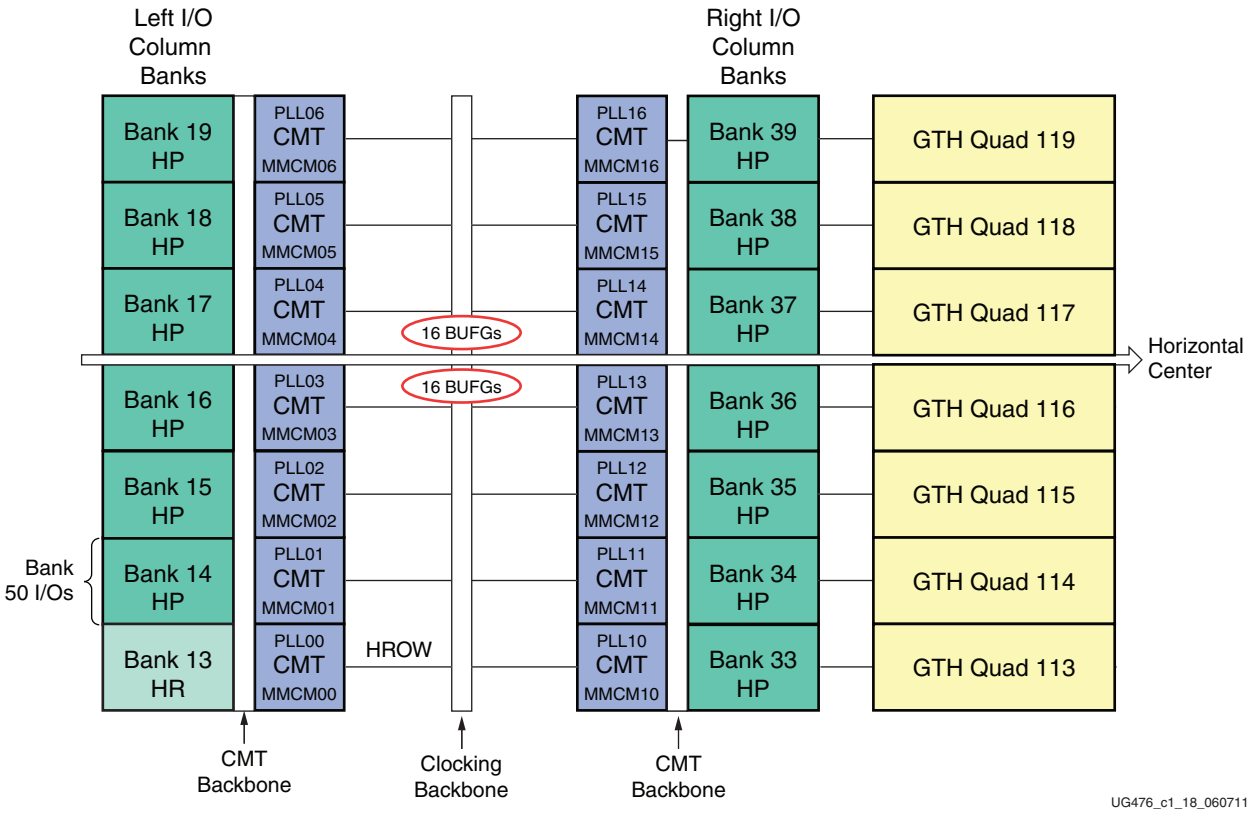

Figure 1-14: **XC7VX330T Banks**

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XC7VX415T Banks

Figure 1-15 shows the I/O and transceiver banks for the XC7VX415T.

FFG1157 Package

- All HP banks are fully bonded out.
- GTH Quads 119, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads are fully bonded out in this package.

FFG1927 Package

All HP banks and the GTH Quads are fully bonded out in this package.

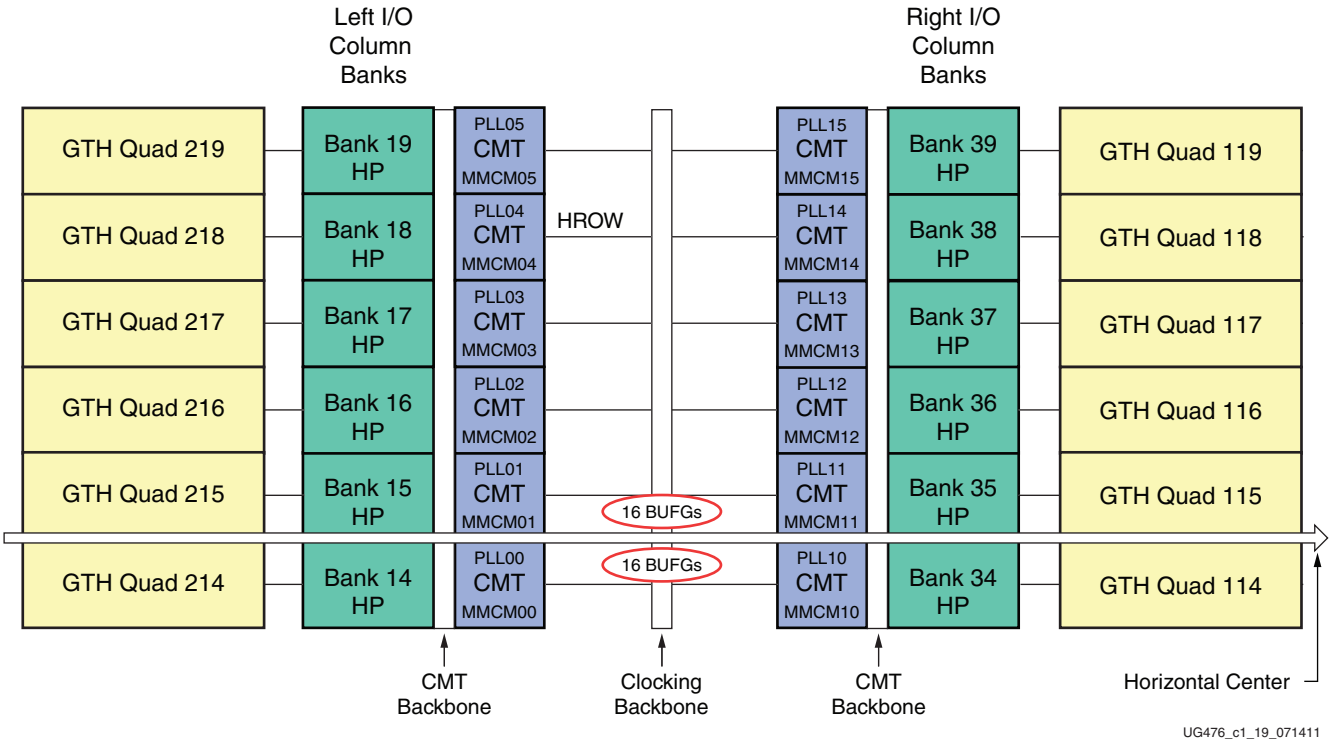

Figure 1-15: **XC7VX415T Banks**

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XC7VX485T Banks

Figure 1-16 shows the I/O and transceiver banks for the XC7VX485T.

FFG1157 Package

- HP banks 13 and 33 are not bonded out.
- GTX Quads 113, 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP banks 13, 18, 19, 33, 37, 38, and 39 are not bonded out.
- GTX Quads 113 and 213 are not bonded out.

FFG1761 Package

- All HP banks are fully bonded out in this package.
- GTX Quads 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1927 Package

- HP banks 13 and 33 are not bonded out.
- All the GTX Quads are fully bonded out in this package.

FFG1930 Package

- All HP banks are fully bonded out in this package.
- GTX Quads 119, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

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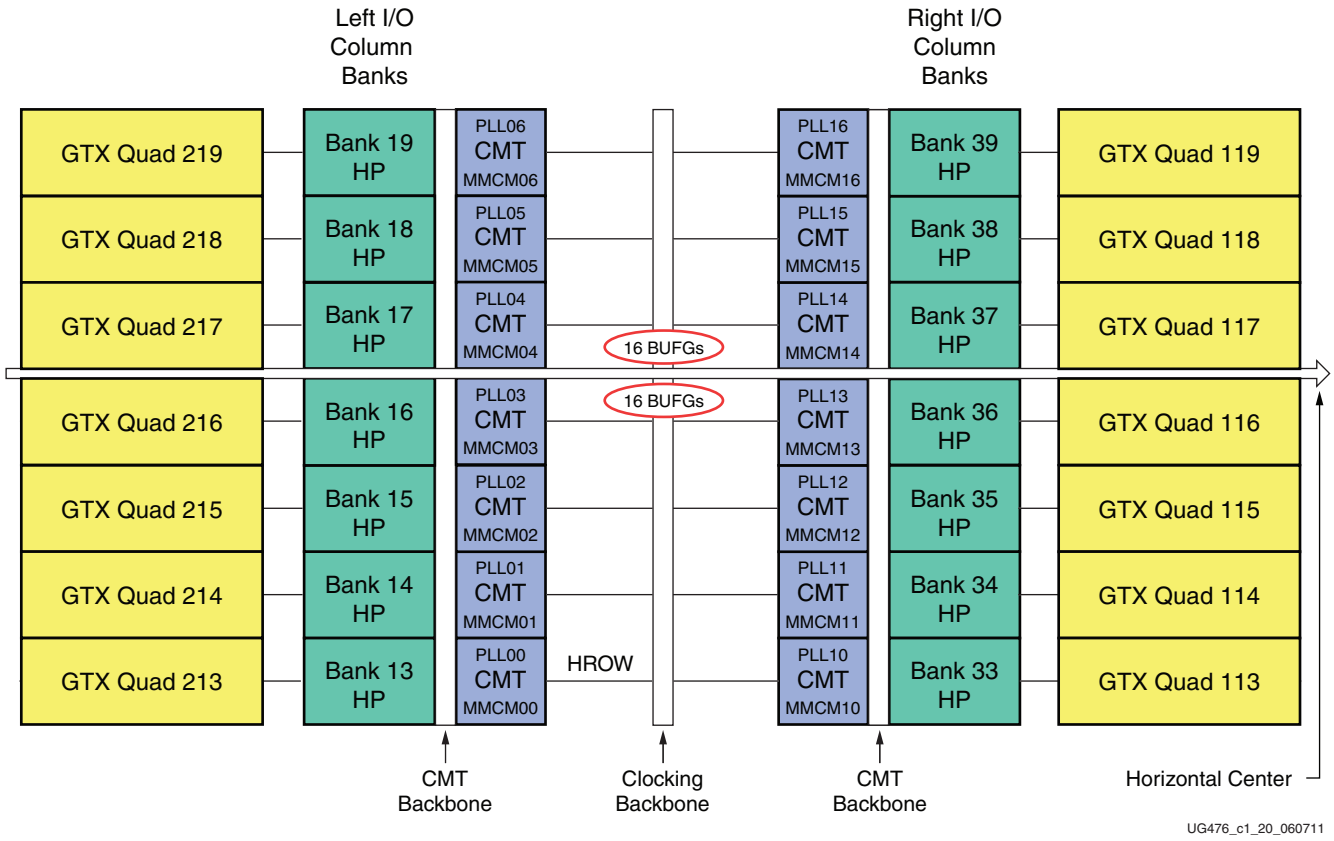

Figure 1-16: **XC7VX485T Banks**

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XC7VX550T Banks

Figure 1-17 shows the I/O and transceiver banks for the XC7VX550T.

FFG1158 Package

- HP banks 12, 13, 18, 19, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 112, 113, 212, and 213 are not bonded out.

FFG1927 Package

- HP banks 12, 13, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

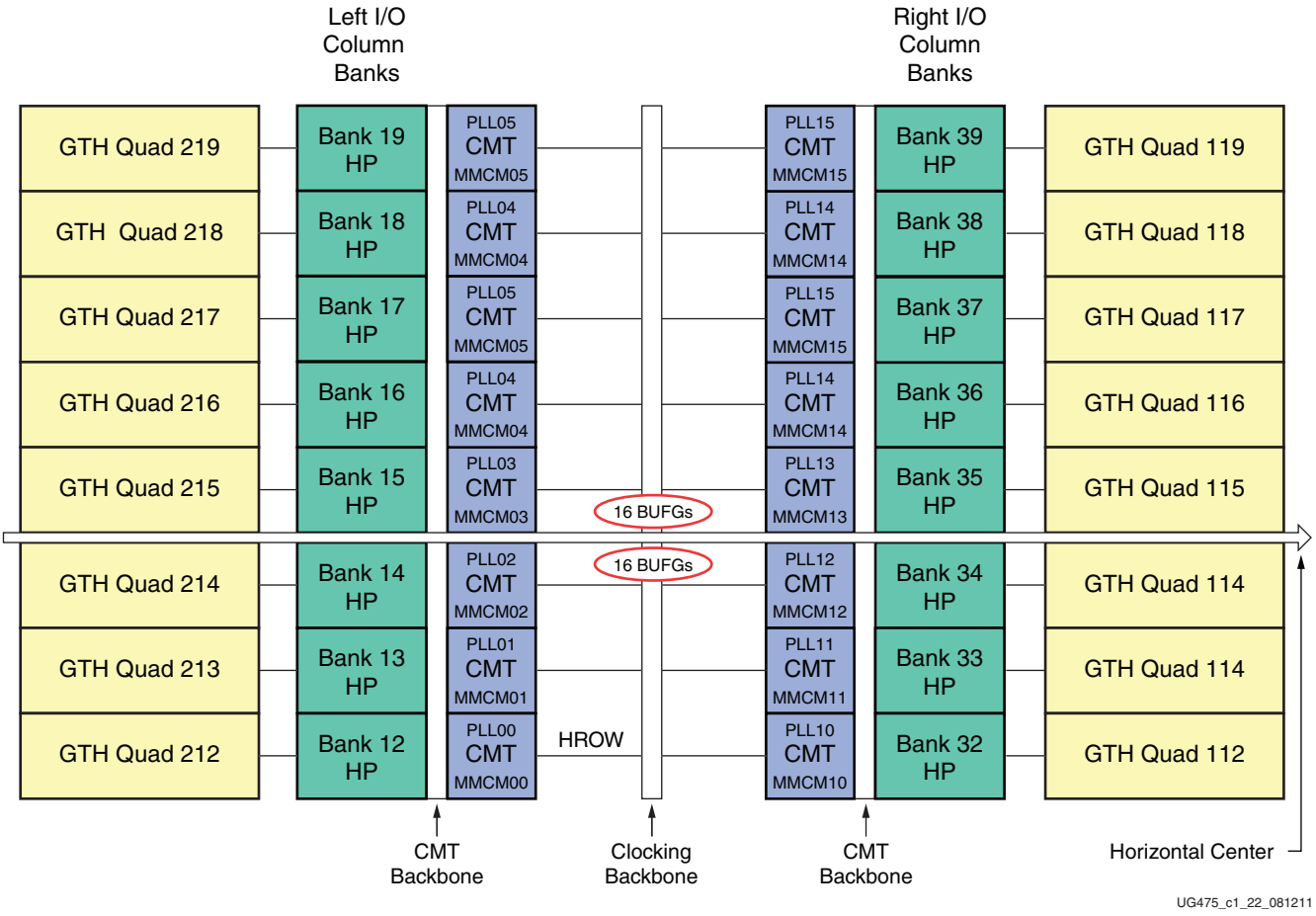

Figure 1-17: **XC7VX550T Banks**

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XC7VX690T Banks

Figure 1-18 shows the I/O and transceiver banks for the XC7VX690T.

FFG1157 Package

- HP banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- GTH Quads 110, 111, 112, 113, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1158 Package

- HP banks 10, 11, 12, 13, 18, 19, 30, 31, 32, 33, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 111, 112, 113, 210, 211, 212, and 213 are not bonded out.

FFG1761 Package

- HP banks 10, 11, and 30 are not bonded out.
- GTH Quads 110, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

FFG1926 Package

- HP bank 17 is partially bonded out.
- HP banks 18, 19, 37, 38, and 39 are not bonded out.
- GTH Quads 110, 119, 210, and 219 are not bonded out.

FFG1927 Package

- HP banks 10, 11, 12, 13, 30, 31, 32, and 33 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 Package

- All HP banks are fully bonded out in this package.
- GTH Quads 110, 111, 112, 119, 210, 211, 212, 213, 214, 215, 216, 217, 218, and 219 are not bonded out.

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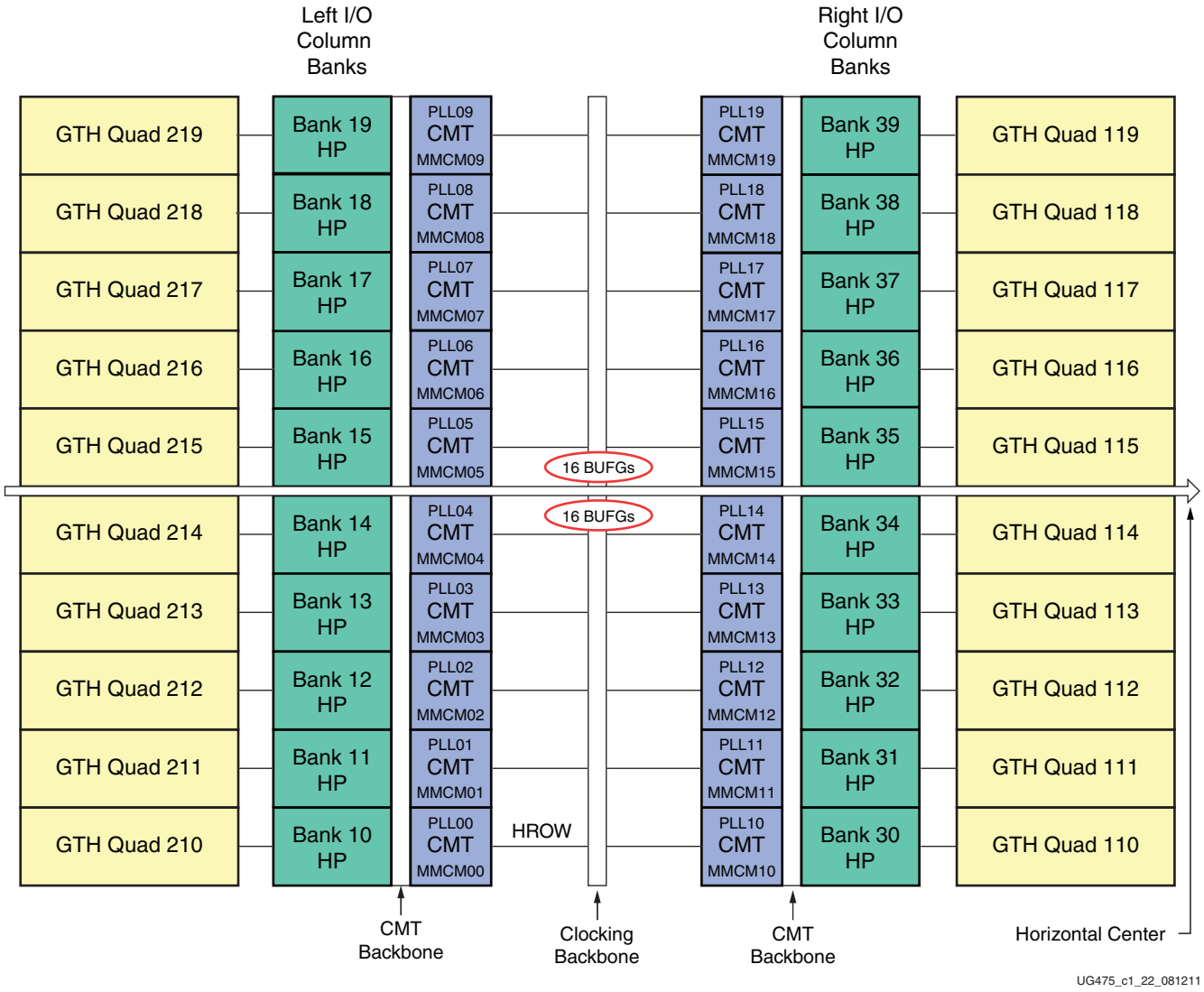

Figure 1-18: **XC7VX690T Banks**

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XC7VX980T Banks

Figure 1-19 shows the I/O and transceiver banks for the XC7VX980T.

FFG1926 Package

- HP bank 17 is partially bonded out.
- HP banks 18, 37, and 38 are not bonded out.
- GTH Quads 110 and 210 are not bonded out.

FFG1928 Package

- HP bank 16 is partially bonded out.
- HP banks 10, 11, 12, 17, 18, 30, 31, and 32 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FFG1930 Package

- All HP banks are fully bonded out in this package.
- GTH Quads 110, 111, 112, 210, 211, 212, 213, 214, 215, 216, 217, and 218 are not bonded out.

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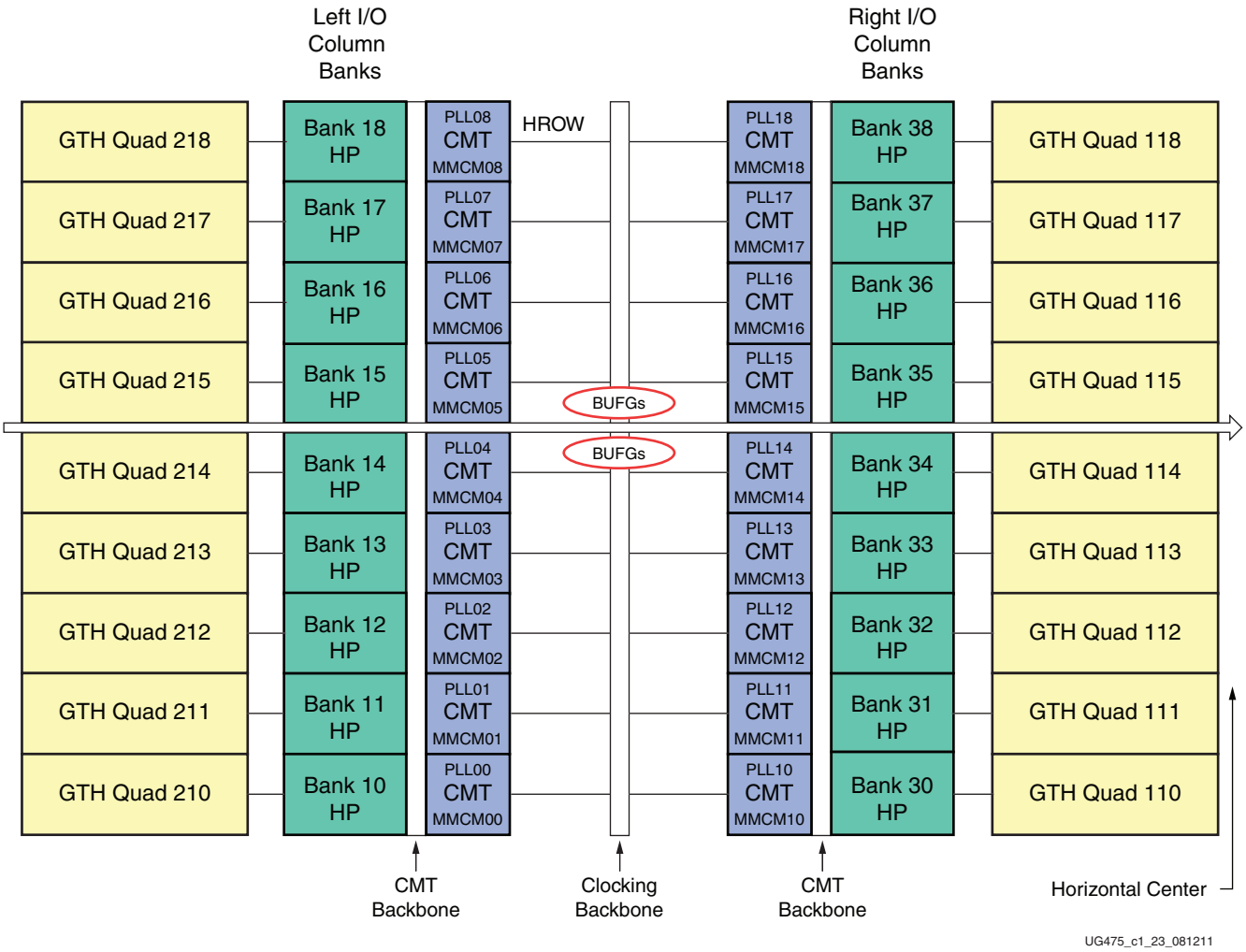

Figure 1-19: **XC7VX980T Banks**

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XC7VX1140T Banks

Figure 1-20 shows the I/O and transceiver banks for the XC7VX1140T.

FLG1928 Package

- HP bank 16 is partially bonded out.
- HP banks 10, 11, 12, 17, 18, 19, 20, 21, 30, 31, 32, 39, 40, and 41 are not bonded out.
- All GTH Quads are fully bonded out in this package.

FLG1930 Package

- HP banks 40 and 41 are not bonded out.
- GTH Quads 110, 111, 112, 119, 120, 121, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, and 221 are not bonded out.

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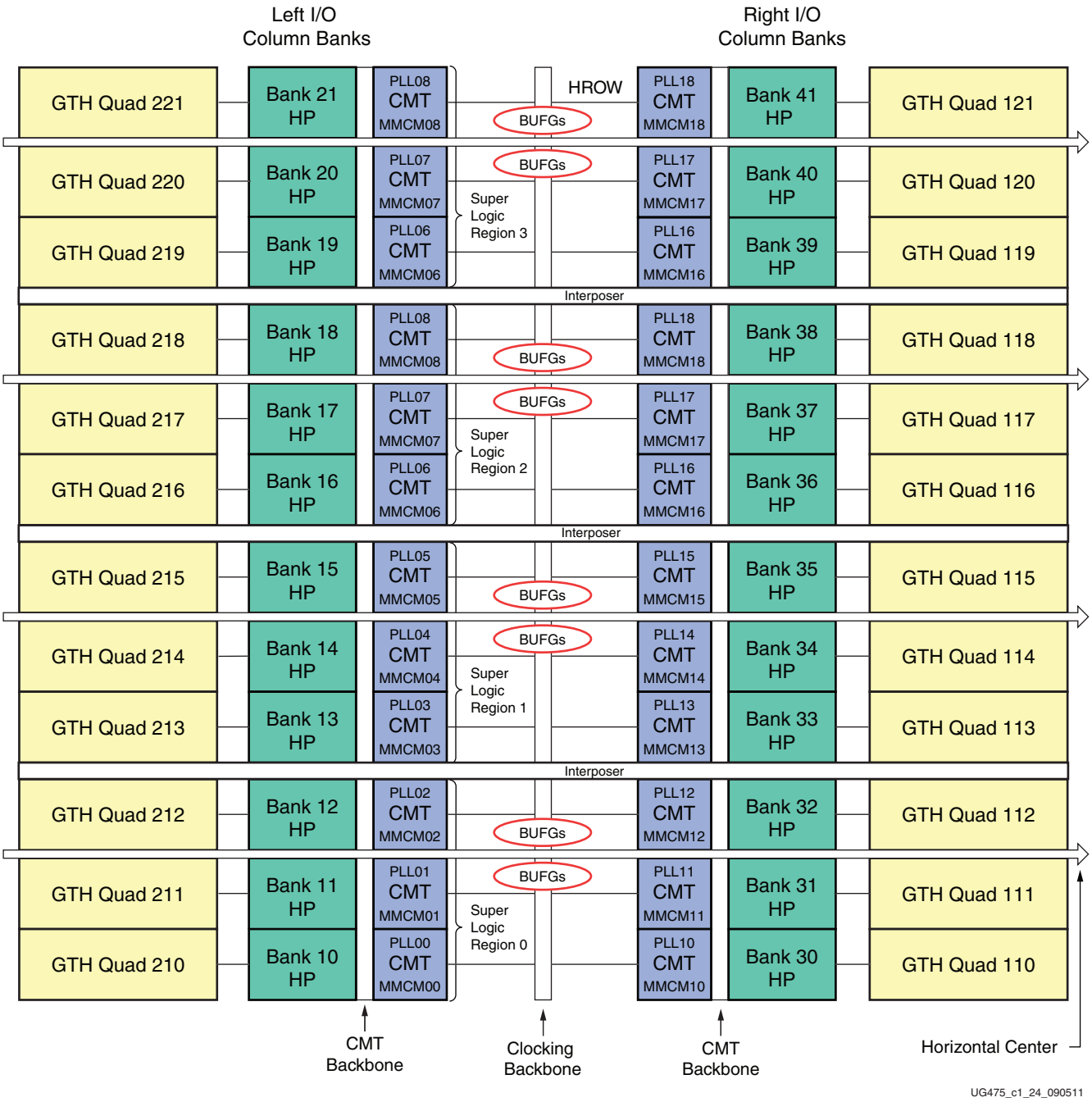

Figure 1-20: **XC7VX1140T Banks**

Note: The figures for some Virtex-7 FPGAs are in development.

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Chapter 2

7 Series FPGAs Package Files

About ASCII Package Files

The ASCII files for each package include a comma-separated-values (CSV) version and a text version optimized for a browser or text editor. Each of the files consists of the following:

- Device/Package name (*FPGA Family—Device—Package*), date and time of creation
- Eight columns containing data for each pin:
  - Pin—Pin location on the package.
  - Pin Name—The name of the assigned pin.
  - Memory Byte Group—Memory byte group between 0 and 3. For more information on the memory byte group, see UG586, *7 Series FPGAs Memory Interface Solutions User Guide*.
  - Bank—Bank number.
  - V_{CCAUX} Group—Number corresponding to the V_{CCAUX_IO} power supply for the given pin. V_{CCAUX} is shown for packages with only one V_{CCAUX} group.
  - Super Logic Region—Number corresponding to the super logic region (SLR) in the devices implemented with stacked silicon interconnect (SSI) technology.
  - I/O Type—CONFIG, HR, HP, or GT (GTP, GTX, GTH, GTZ) depending on the I/O type. For more information on the I/O type, see UG471, *7 Series FPGAs SelectIO Resources User Guide*.
  - No-Connect—This list of devices is used for migration between devices that have the same package size and are not connected at that specific pin.
- Total number of pins in the package.

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ASCII Pinout Files

This chapter includes the pinout information tables for the following device/packages.

Note: All package files are ASCII files in TXT and CSV file format.

To download all available Artix-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/artix-7-pkgs.htm

Note: Only the available files listed in Table 2-1 are linked and consolidated in the above ZIP file.

Table 2-1: **Artix-7 FPGAs Package/Device Pinout Files**

Device	CPG236	CSG225	CSG324	FTG256	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A8	CPG236		CSG324	FTG256					
XC7A15	CPG236		CSG324	FTG256					
XC7A30T		CSG225	CSG324	FTG256	FGG484				
XC7A50T		CSG225	CSG324	FTG256	FGG484				
XC7A100T			CSG324	FTG256	FGG484	FGG676			
XC7A200T							FBG484	FBG676	
XC7A350T							FBG484	FBG676	FFG1156

To download all available Kintex-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/kintex-7-pkgs.htm

Table 2-2: **Kintex-7 FPGAs Package/Device Pinout Files**

Device	FB(G)484	FB(G)676	FB(G)900	FF(G)676	FF(G)900	FF(G)901	FF(G)1156
XC7K70T	FBG484	FBG676					
XC7K160T	FB484/ FBG484	FB676/ FBG676		FF676/ FFG676			
XC7K325T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K355T						FF901/ FFG901	
XC7K410T		FB676/ FBG676	FB900/ FBG900	FF676/ FFG676	FF900/ FFG900		
XC7K420T						FF901/ FFG901	FF1156/ FFG1156
XC7K480T						FF901/ FFG901	FF1156/ FFG1156

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To download all available Virtex-7 FPGAs package/device/pinout files click here:

http://www.xilinx.com/support/packagefiles/virtex-7-pkgs.htm

Note: Only the available files listed in Table 2-3 are linked and consolidated in the above ZIP file.

Table 2-3: **Virtex-7 FPGAs Package/Device Pinout Files**

Device	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FL(G)	FL(G)	FL(G)	FL(G)	FH(G)
	1157	1158	1761	1926	1927	1928	1930	1761	1925	1928	1930	1761
XC7V585T	FF1157/ FFG1157		FF1761/ FFG1761									
XC7V1500T								FL1761/ FLG1761				
XC7V2000T									FL1925/ FLG1925			FH1761/ FHG1761
XC7VX330T	FF1157/ FFG1157		FF1761/ FFG1761									
XC7VX415T	FF1157/ FFG1157	FF1158/ FFG1158			FF1927/ FFG1927							
XC7VX485T	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761		FF1927/ FFG1927		FF1930/ FFG1930					
XC7VX550T		FF1158/ FFG1158			FF1927/ FFG1927							
XC7VX690T	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761	FF1926/ FFG1926	FF1927/ FFG1927		FF1930/ FFG1930					
XC7VX980T				FF1926/ FFG1926		FF1928/ FFG1928	FF1930/ FFG1930					
XC7VX1140T										FL1928/ FLG1928	FL1930/ FLG1930	

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Chapter 3

Device Diagrams

Summary

This chapter provides pinout, I/O bank, high-performance and high-range I/O bank, memory groupings, and power and ground placement diagrams for each 7 series FPGA package/device combination. Some figures for Artix-7 FPGAs and Virtex-7 FPGAs are in development.

- Artix-7 FPGAs Device Diagrams Cross-Reference, page 52
- Kintex-7 FPGAs Device Diagrams Cross-Reference, page 57
- Virtex-7 FPGAs Device Diagrams Cross Reference, page 97

The figures provide a top-view perspective.

The symbols for the multi-function I/O pins are represented by only one of the available pin functions; with precedence (by functionality) in this order:

- ADV_B, FCS_B, FOE_B, MOSI, FWE_B, DOUT_CSO_B, CSI_B, PUDC_B, or RDWR_B
- RS0–RS1
- AD0P/AD0N–AD15P/AD15N
- EMCCLK
- VRN, VRP, or VREF
- D00–D31
- A00–A28
- DQS, MRCC, or SRCC

For example, a pin description such as IO_L8P_SRCC_12 is represented with a SRCC symbol, a pin description such as IO_L19N_T3_A09_D25_VREF_14 is represented with a VREF symbol, and a pin description such as IO_L21N_T3_DQS_A06_D22_14 is represented with a D0–D31 symbol.

Note: The available files are listed in Table 3-1, Table 3-2, and Table 3-3 are linked. Figures for some Artix-7 FPGAs and Virtex-7 FPGAs are in development.

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Artix-7 FPGAs Device Diagrams

Table 3-1: **Artix-7 FPGAs Device Diagrams Cross-Reference**

Device	CPG236	CSG225	CSG324	FTG256	FGG484	FGG676	FBG484	FBG676	FFG1156
XC7A8			page 52						
XC7A15			page 52						
XC7A30T			page 55						
XC7A50T			page 55						
XC7A100T			page 55						
XC7A200T									
XC7A350T									

Note: The available files are listed in Table 3-1 are linked. Figures for some Artix-7 FPGAs are in development.

CSG324 Package—XC7A8 and XC7A15

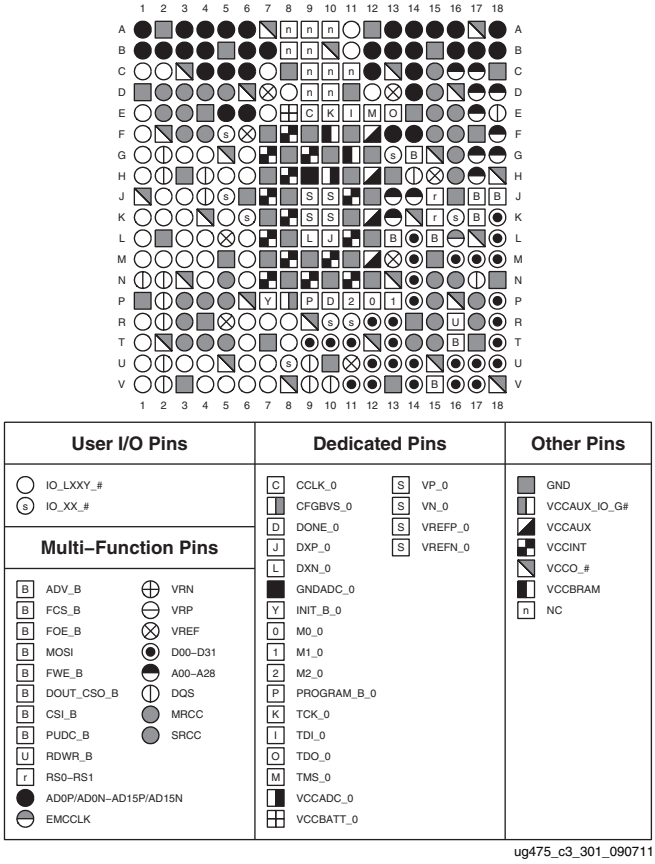

Figure 3-1: **CSG324 Package—XC7A8 and XC7A15 Pinout Diagram**

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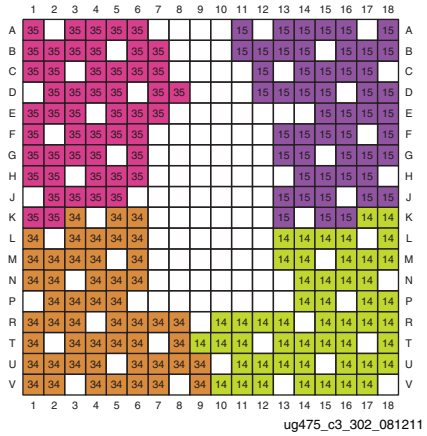

Figure 3-2: **CSG324 Package—XC7A8 and XC7A15 I/O Banks**

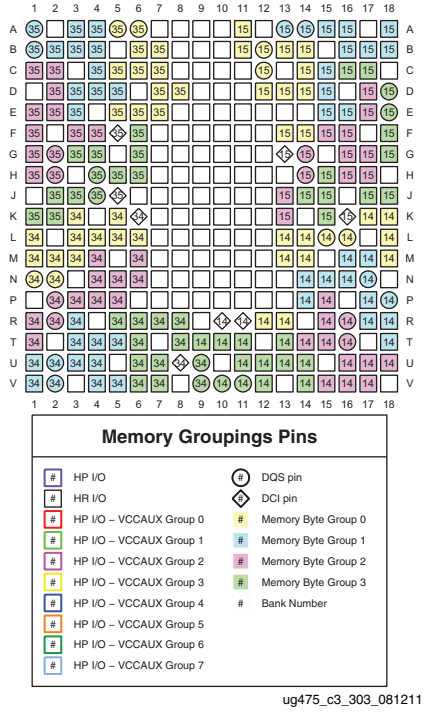

Figure 3-3: **CSG324 Package—XC7A8 and XC7A15 Memory Groupings**

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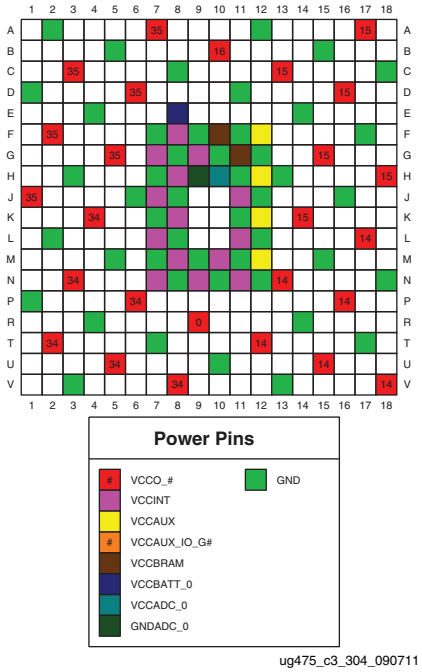

Figure 3-4: **CSG324 Package—XC7A8 and XC7A15 Power and GND Placement**

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CSG324 Package—XC7A30T, XC7A50T, and XC7A100T

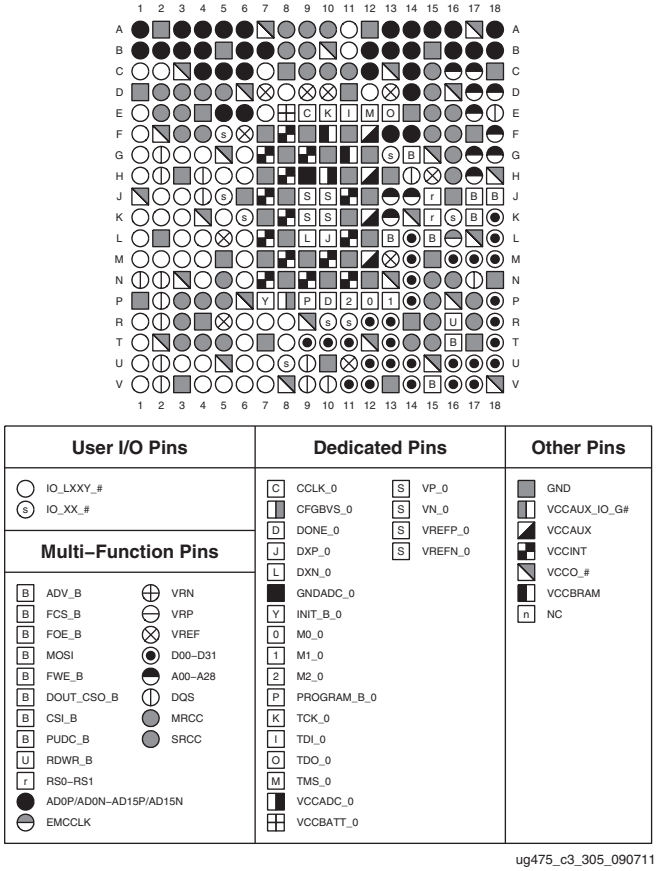

Figure 3-5: **CSG324 Package—XC7A30T, XC7A50T, and XC7A100T Pinout Diagram**

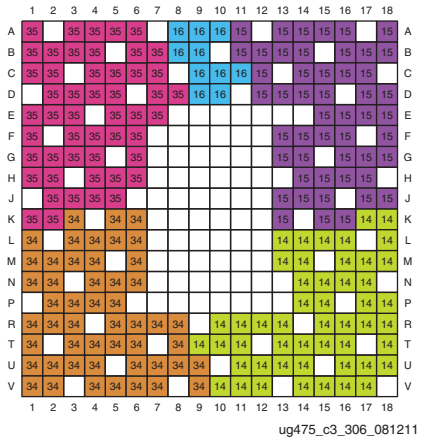

Figure 3-6: **CSG324 Package—XC7A30T, XC7A50T, and XC7A100T I/O Banks**

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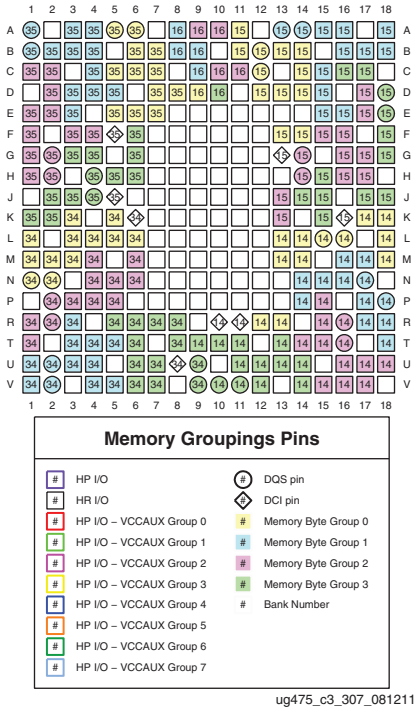

Figure 3-7: **CSG324 Package—XC7A30T, XC7A50T, and XC7A100T Memory Groupings**

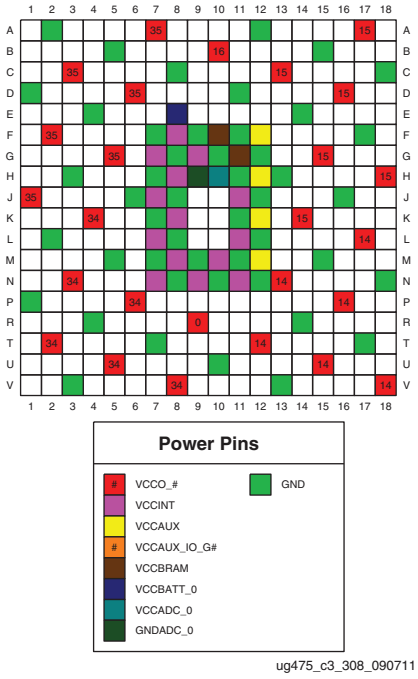

Figure 3-8: **CSG324 Package—XC7A30T, XC7A50T, and XC7A100T Power and GND Placement**

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Kintex-7 FPGAs Device Diagrams

Table 3-2: **Kintex-7 FPGAs Device Diagrams Cross-Reference**

Device	FB(G)484	FB(G)676	FB(G)900	FF(G)676	FF(G)900	FF(G)901	FF(G)1156
XC7K70T	page 57	page 60					
XC7K160T	page 57	page 63		page 70			
XC7K325T		page 63	page 66	page 70	page 73		
XC7K355T						page 77	
XC7K410T		page 63	page 66	page 70	page 73		
XC7K420T						page 81	page 89
XC7K480T						page 85	page 93

FBG484 Package—XC7K70T and XC7K160T

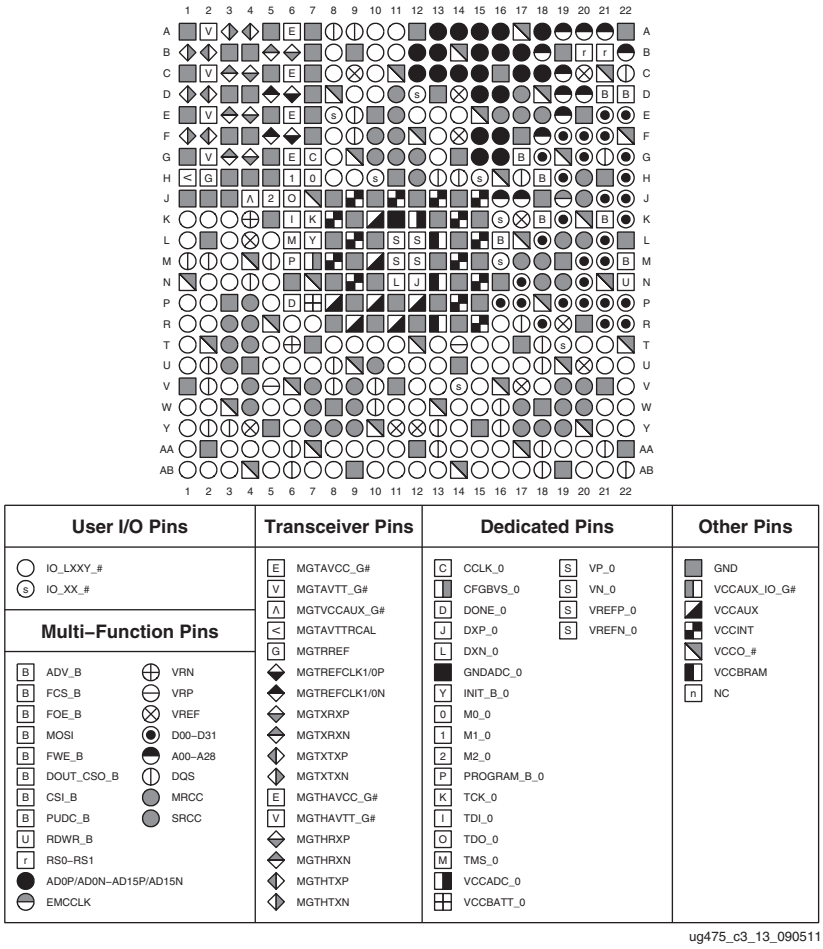

Figure 3-9: **FBG484 Package—XC7K70T and XC7K160T Pinout Diagram**

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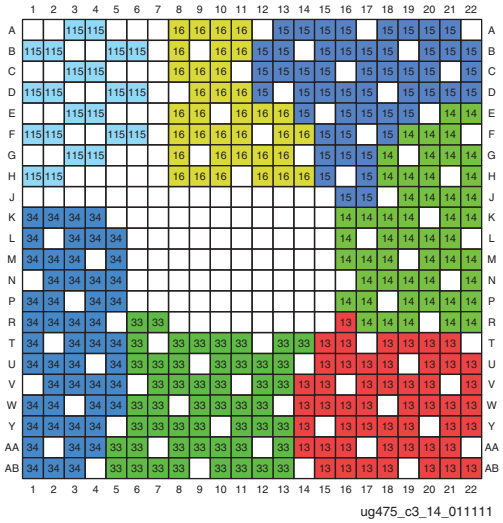

Figure 3-10: **FBG484 Package—XC7K70T and XC7K160T I/O Banks**

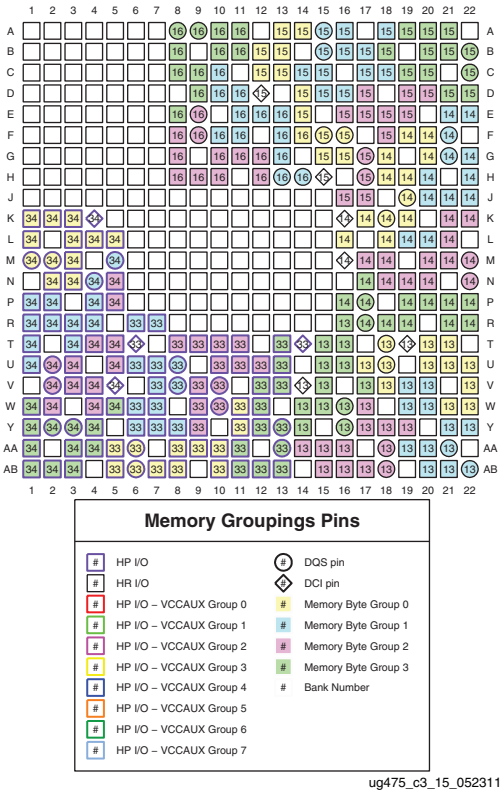

Figure 3-11: **FBG484 Package—XC7K70T and XC7K160T Memory Groupings**

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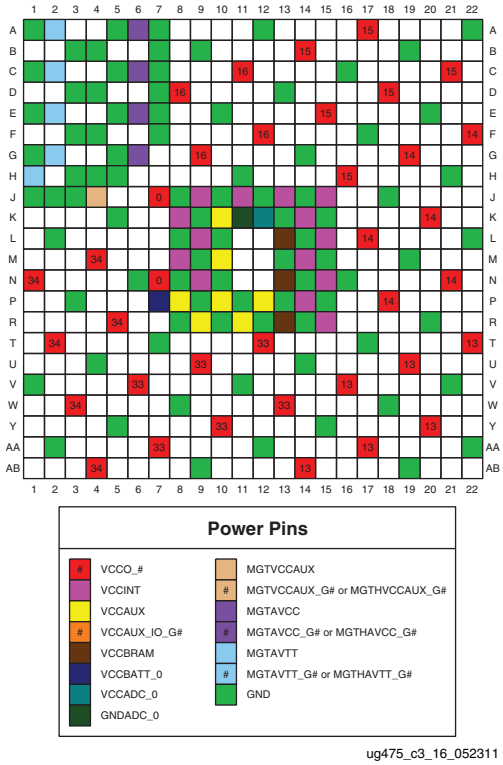

Figure 3-12: **FBG484 Package—XC7K70T and XC7K160T Power and GND Placement**

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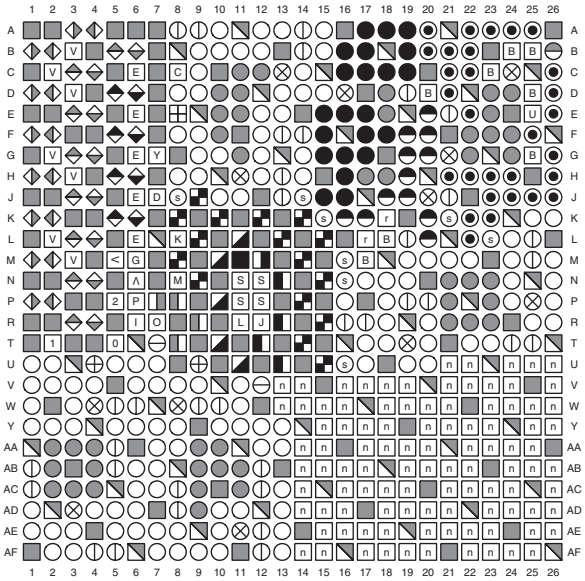
FBG676 Package—XC7K70T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	VRN	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	VRP	MGTRREF	DXN_0	VCCO_#
FOE_B	VREF	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	D00–D31	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	A00–A28	MGTXRXP	M0_0
DOUT_CSO_B	DQS	MGTXRXN	M1_0
CSI_B	MRCC	MGTXTXP	M2_0
PUDC_B	SRCC	MGTXTXN	PROGRAM_B_0
RDWR_B	MGTHAVCC_G#	TCK_0
RS0–RS1	MGTHAVTT_G#	TDI_0
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0
EMCCLK	MGTHRXN	TMS_0
	MGTHTXP	VCCADC_0
	MGTHTXN	VCCBATT_0

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Figure 3-13: **FBG676 Package—XC7K70T Pinout Diagram**

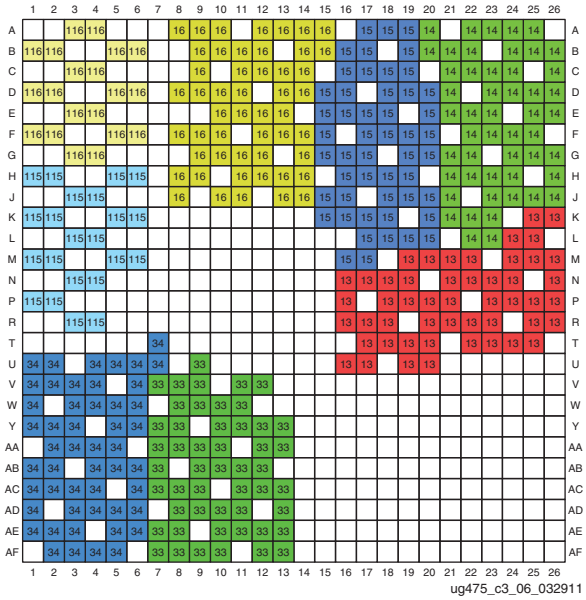

Figure 3-14: **FBG676 Package—XC7K70T I/O Banks**

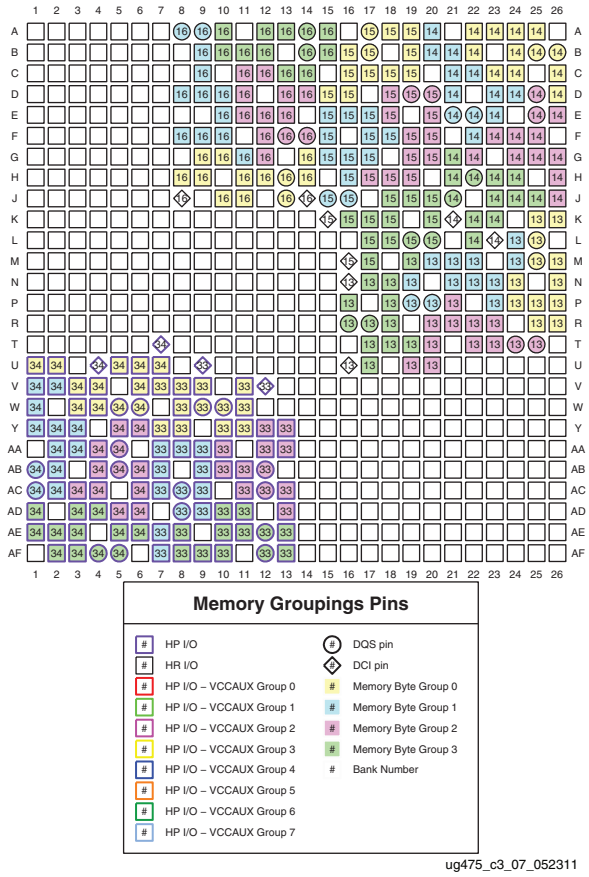

Figure 3-15: **FBG676 Package—XC7K70T Memory Groupings**

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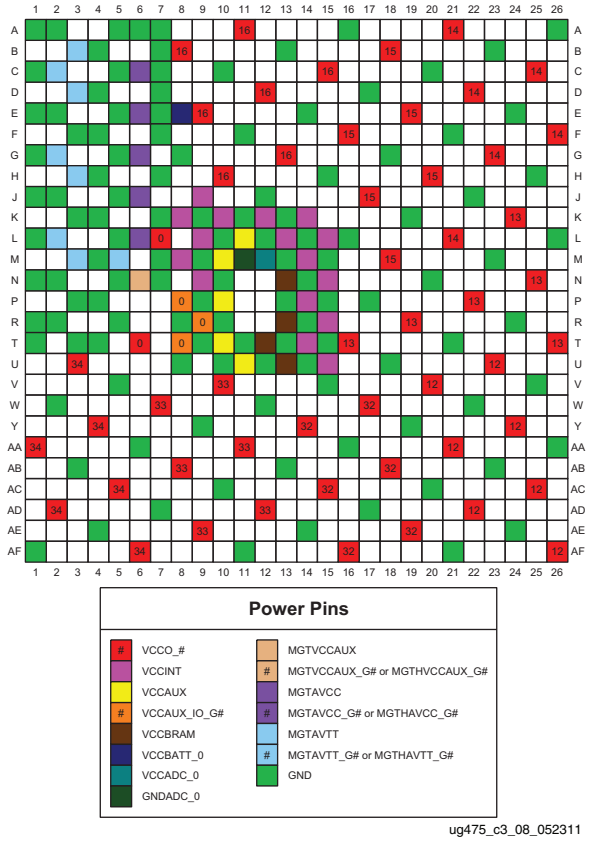

Figure 3-16: **FBG676 Package—XC7K70T Power and GND Placement**

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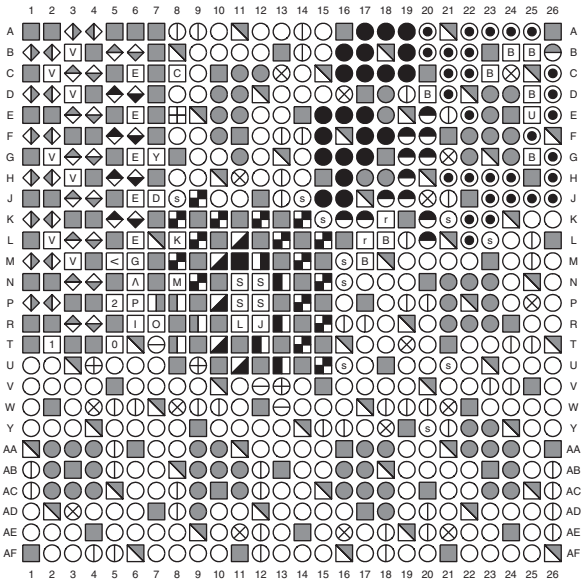
FBG676 Package—XC7K160T, XC7K325T, and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-17: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

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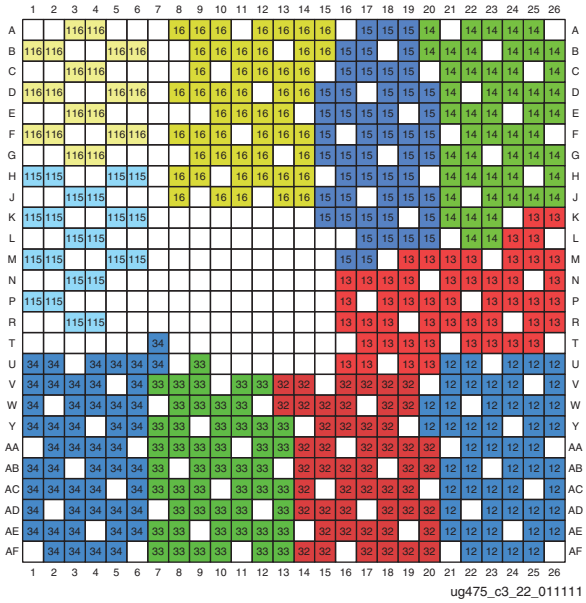

Figure 3-18: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

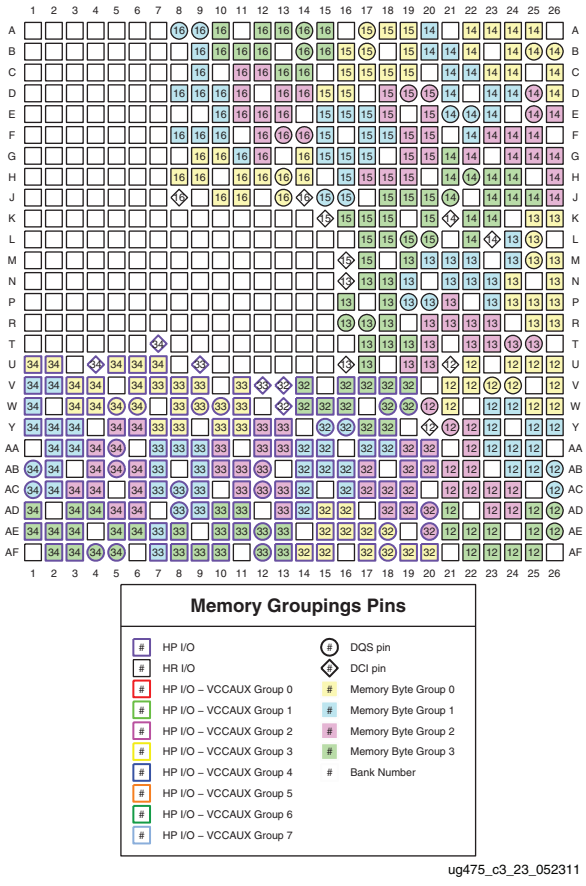

Figure 3-19: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

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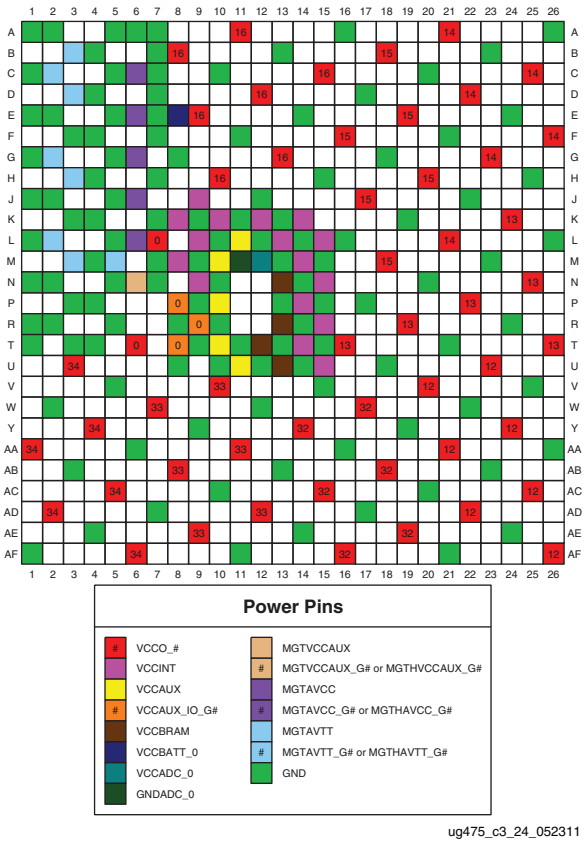

Figure 3-20: **FBG676 Package—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

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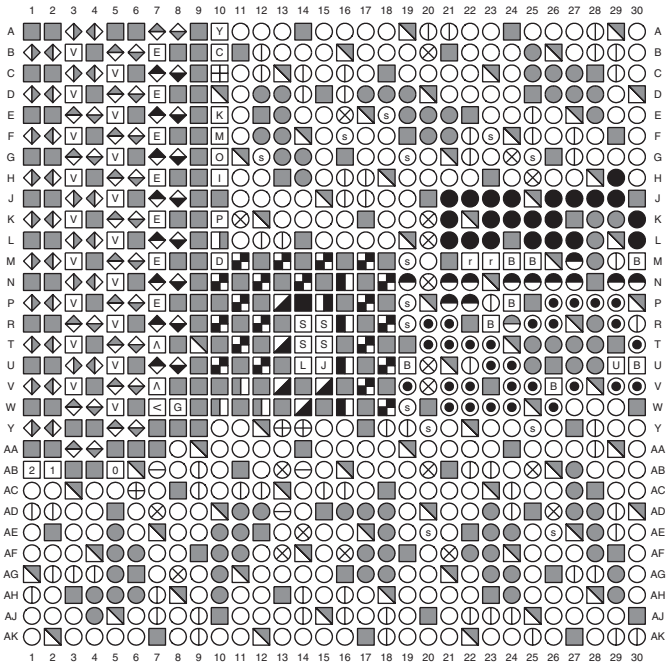
FBG900 Package—XC7K325T and XC7K410T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VCCAUX
ADV_B	MGTAVTTRCAL	DXP_0	VCCINT
FCS_B	MGTRREF	DXN_0	VCCO_#
FOE_B	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	MGTXRXP	M0_0	
DOUT_CSO_B	MGTXRXN	M1_0	
CSI_B	MGTXTXP	M2_0	
PUDC_B	MGTXTXN	PROGRAM_B_0	
RDWR_B	MGTHAVCC_G#	TCK_0	
RS0–RS1	MGTHAVTT_G#	TDI_0	
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0	
EMCCLK	MGTHRXN	TMS_0	
VRN	MGTHTXP	VCCADC_0	
VRP	MGTHTXN	VCCBATT_0	
VREF		VP_0	
D00–D31		VN_0	
A00–A28		VREFP_0	
DQS		VREFN_0	
MRCC			
SRCC			

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Figure 3-21: **FBG900 Package—XC7K325T and XC7K410T Pinout Diagram**

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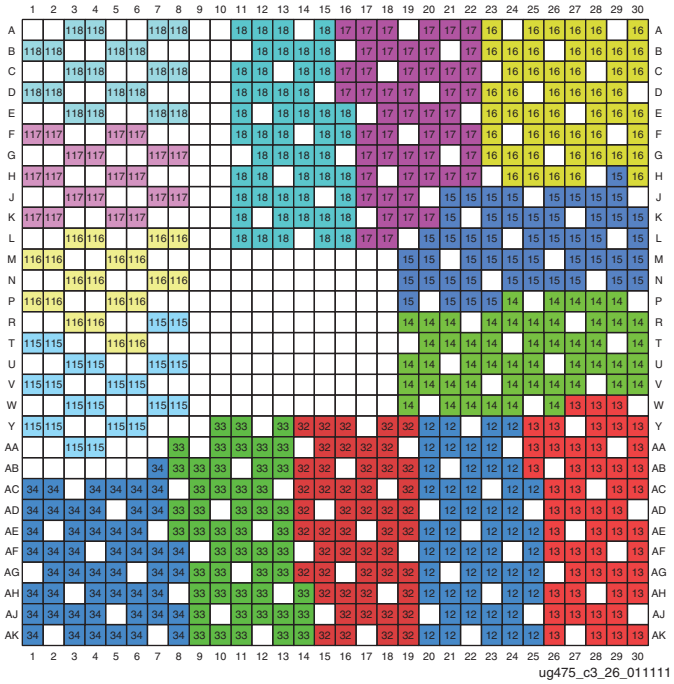

Figure 3-22: **FBG900 Package—XC7K325T and XC7K410T I/O Banks**

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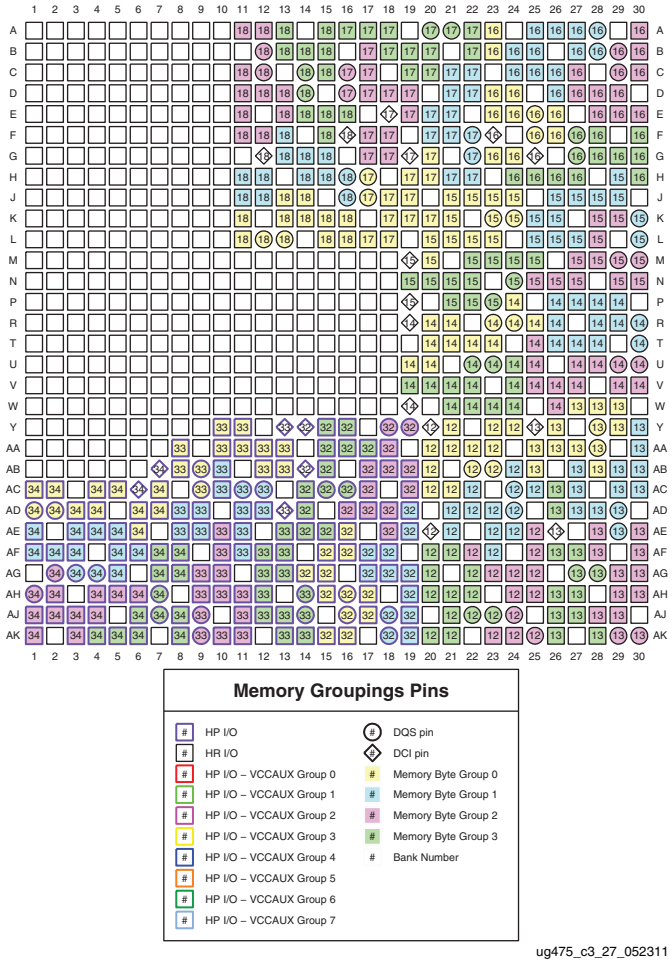


Figure 3-23: **FBG900 Package—XC7K325T and XC7K410T Memory Groupings**

www.BDTIC.com/XILINX

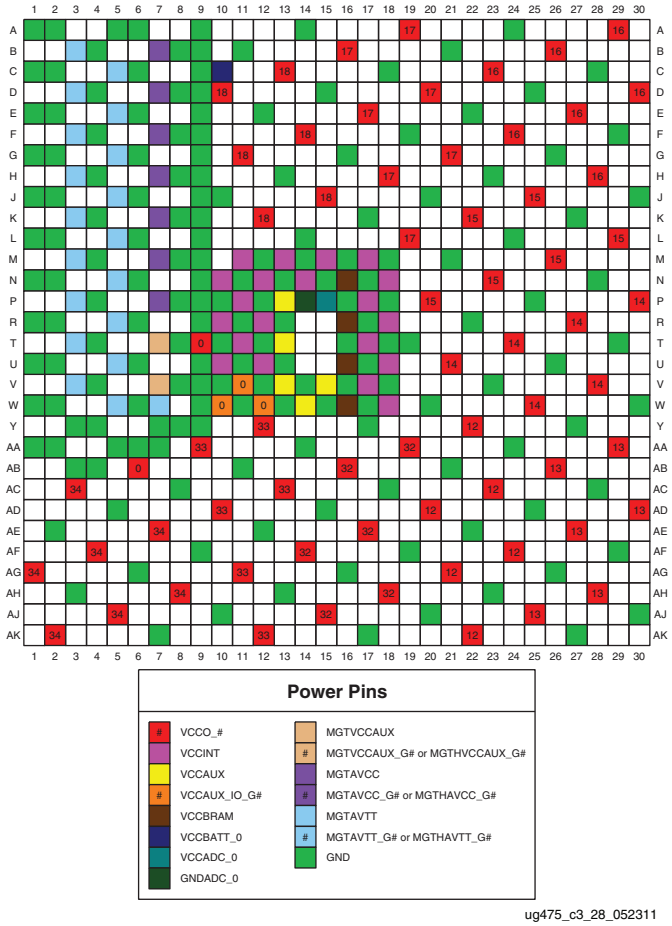


Figure 3-24: **FBG900 Package—XC7K325T and XC7K410T Power and GND Placement**

www.BDTIC.com/XILINX

FFG676 Package—XC7K160T, XC7K325T, and XC7K410T

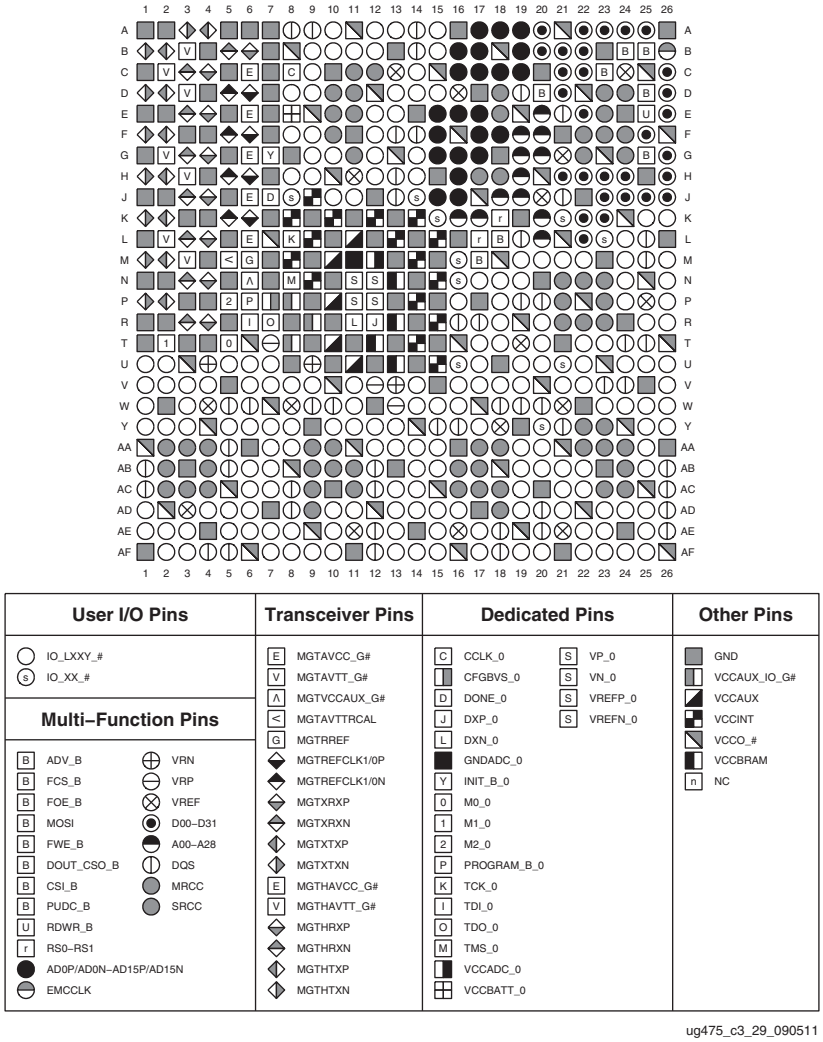


Figure 3-25: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Pinout Diagram**

www.BDTIC.com/XILINX

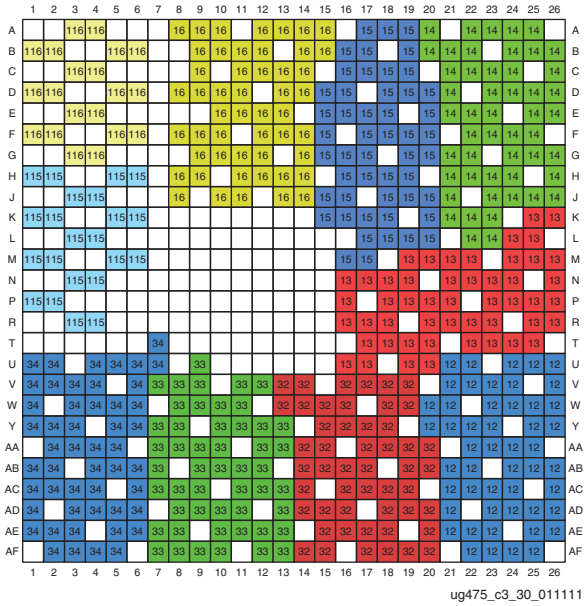


Figure 3-26: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T I/O Banks**

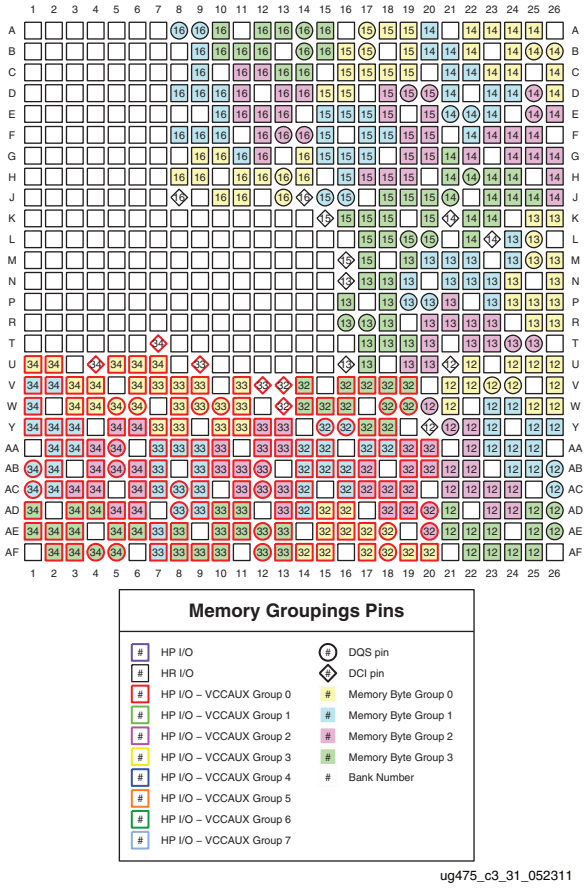


Figure 3-27: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Memory Groupings**

www.BDTIC.com/XILINX

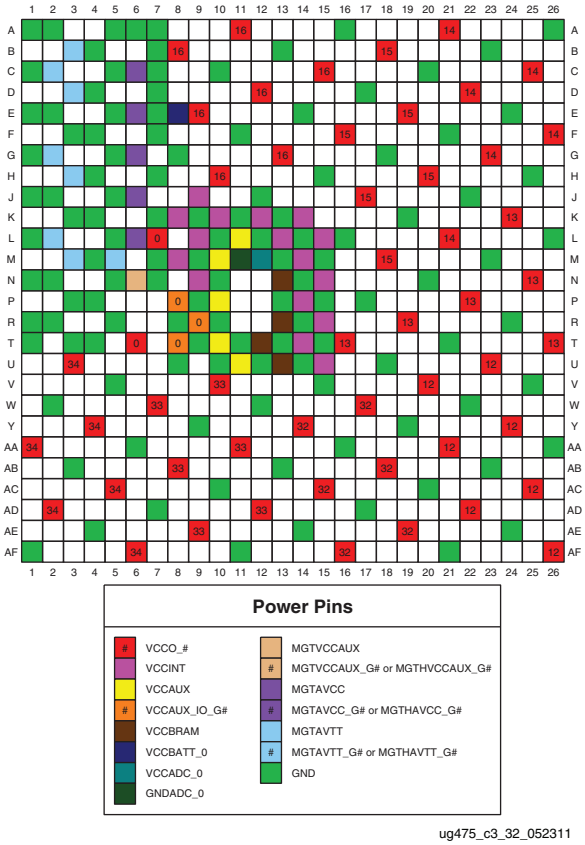
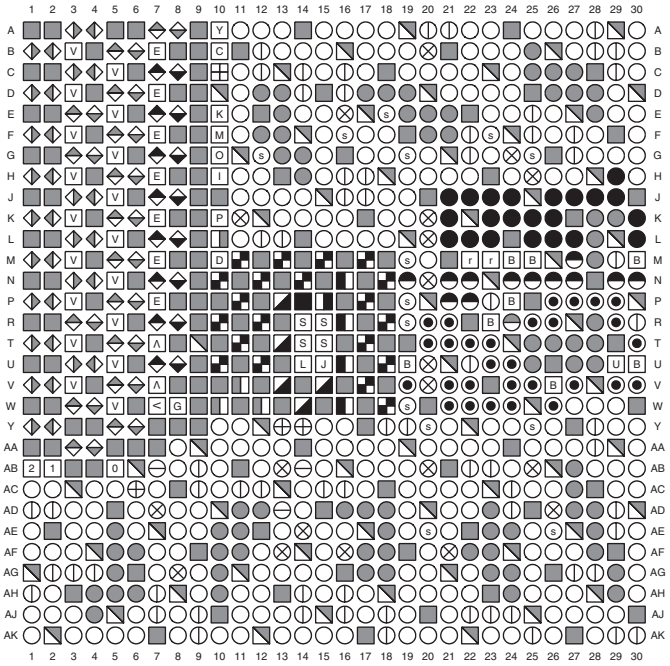


Figure 3-28: **FFG676 Package—XC7K160T, XC7K325T, and XC7K410T Power and GND Placement**

www.BDTIC.com/XILINX
www.xilinx.com

FFG900 Package—XC7K325T and XC7K410T



User I/O Pins		Transceiver Pins	Dedicated Pins		Other Pins
IO_LXXY_#		MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#		MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins		MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	VRN	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	VRP	MGTRREF	DXN_0		VCCO_#
FOE_B	VREF	MGTREFCLK1/0P	GNDADC_0		VCCBRAM
MOSI	D00–D31	MGTREFCLK1/0N	INIT_B_0		NC
FWE_B	A00–A28	MGTXRXP	M0_0		
DOUT_CSO_B	DQS	MGTXRXN	M1_0		
CSI_B	MRCC	MGTXTXP	M2_0		
PUDC_B	SRCC	MGTXTXN	PROGRAM_B_0		
RDWR_B		MGTHAVCC_G#	TCK_0		
RS0–RS1		MGTHAVTT_G#	TDI_0		
AD0P/AD0N–AD15P/AD15N		MGTHRXP	TDO_0		
EMCCLK		MGTHRXN	TMS_0		
		MGTHTXP	VCCADC_0		
		MGTHTXN	VCCBATT_0		

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Figure 3-29: **FFG900 Package—XC7K325T and XC7K410T Pinout Diagram**

www.BDTIC.com/XILINX

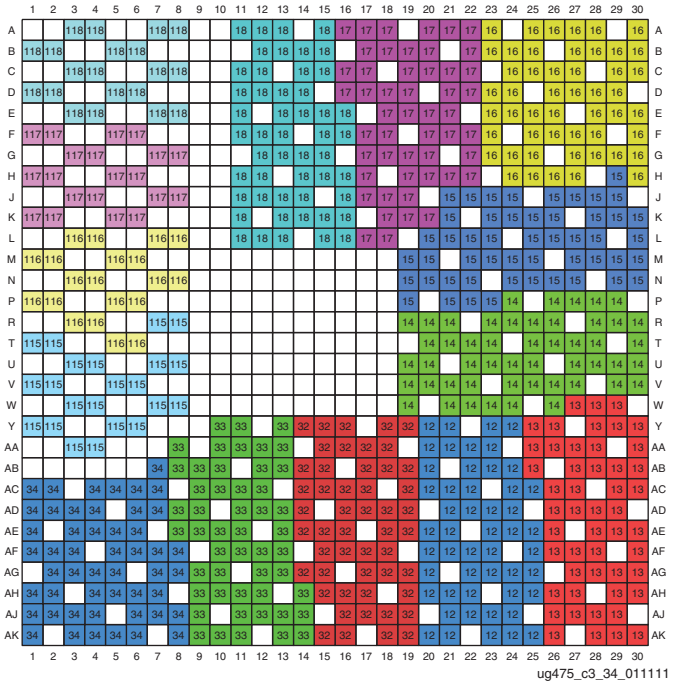


Figure 3-30: **FFG900 Package—XC7K325T and XC7K410T I/O Banks**

www.BDTIC.com/XILINX

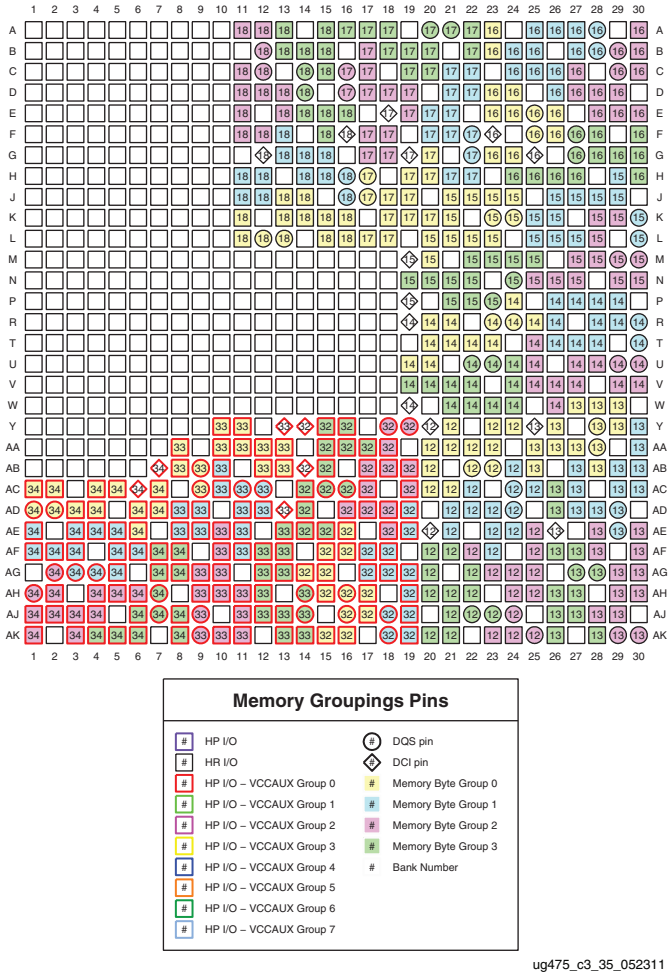


Figure 3-31: **FFG900 Package—XC7K325T and XC7K410T Memory Groupings**

www.BDTIC.com/XILINX

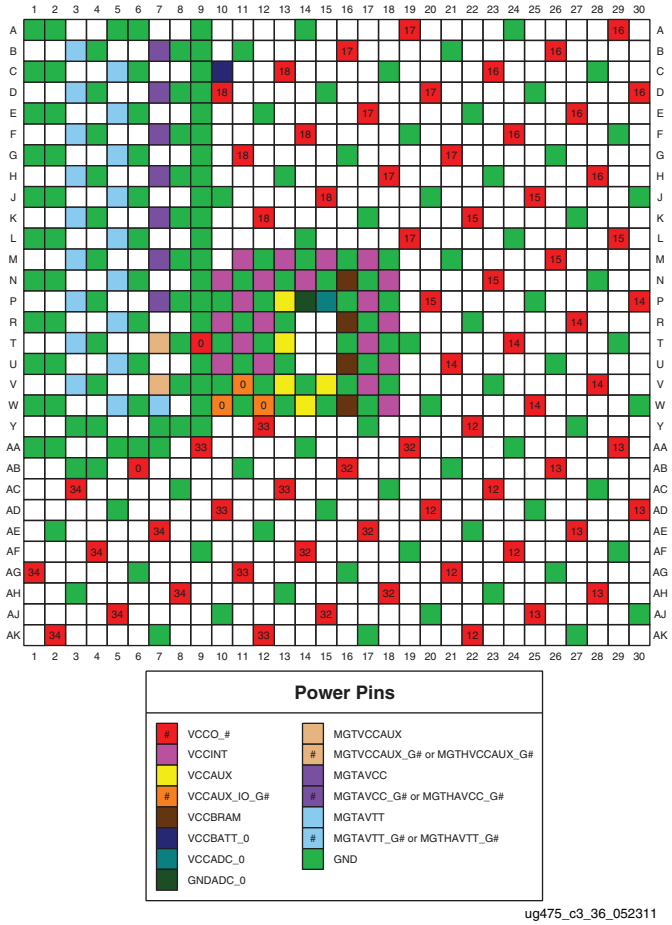


Figure 3-32: **FFG900 Package—XC7K325T and XC7K410T Power and GND Placement**

www.BDTIC.com/XILINX

FFG901 Package—XC7K355T

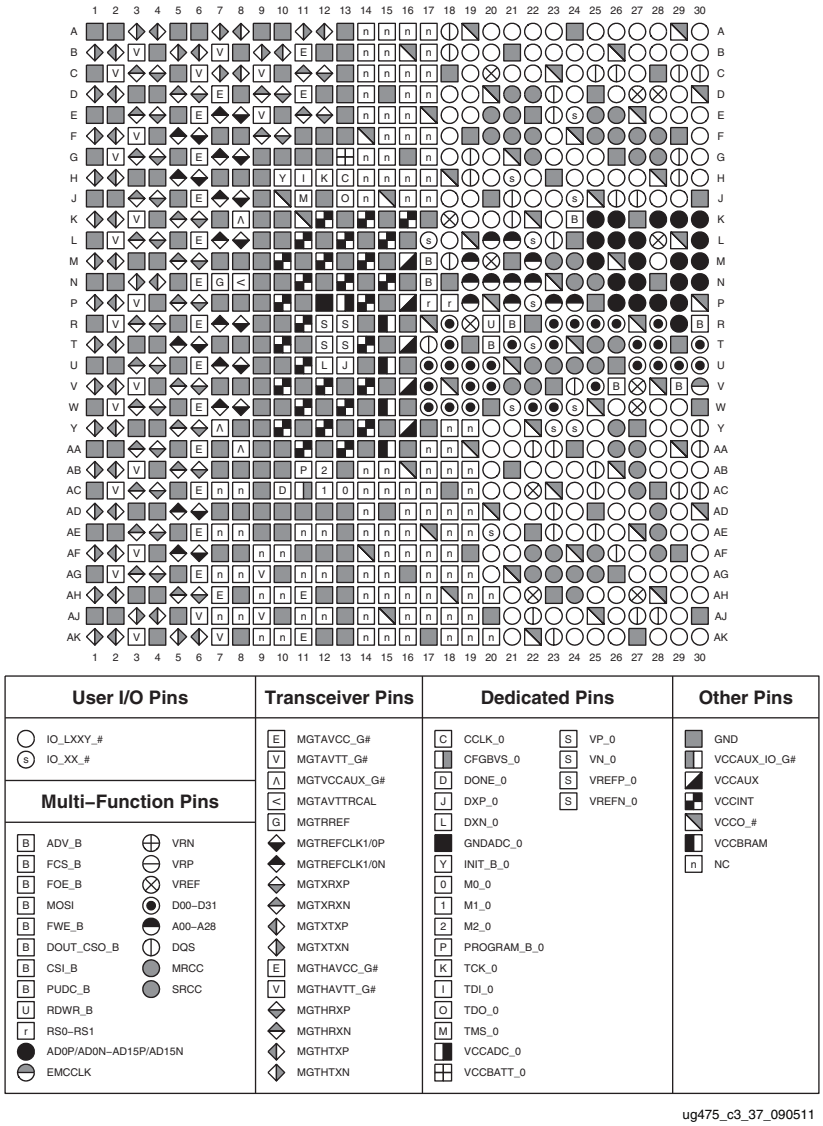


Figure 3-33: **FFG901 Package—XC7K355T Pinout Diagram**

www.BDTIC.com/XILINX

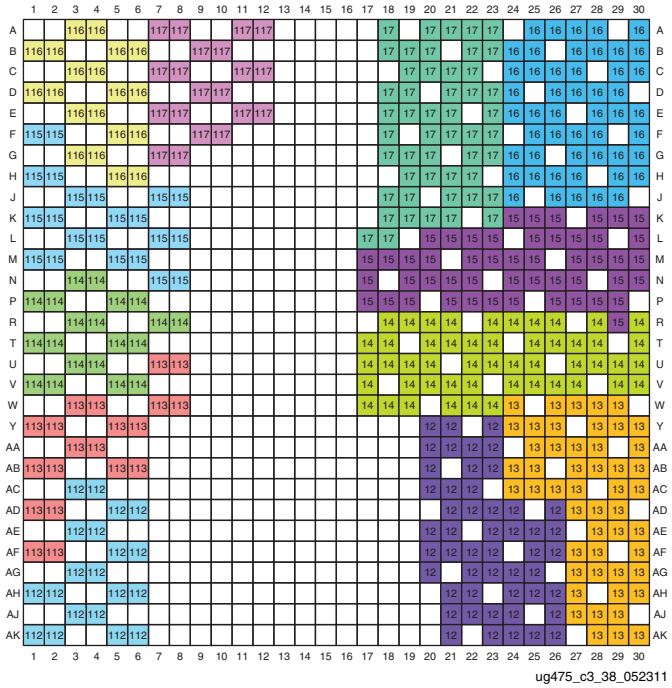


Figure 3-34: **FFG901 Package—XC7K355T I/O Banks**

www.BDTIC.com/XILINX

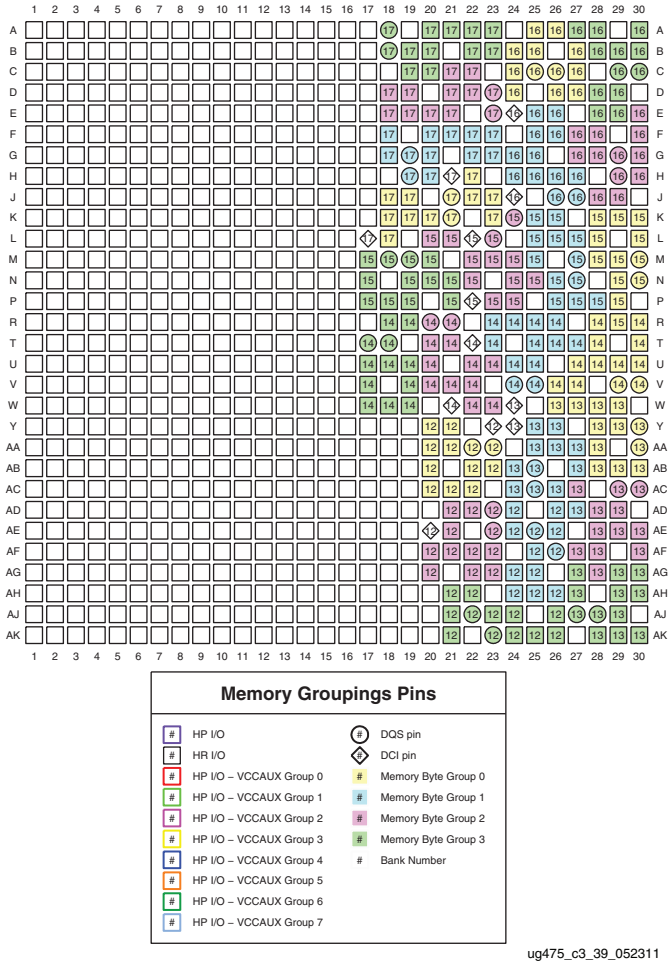


Figure 3-35: **FFG901 Package—XC7K355T Memory Groupings**

www.BDTIC.com/XILINX

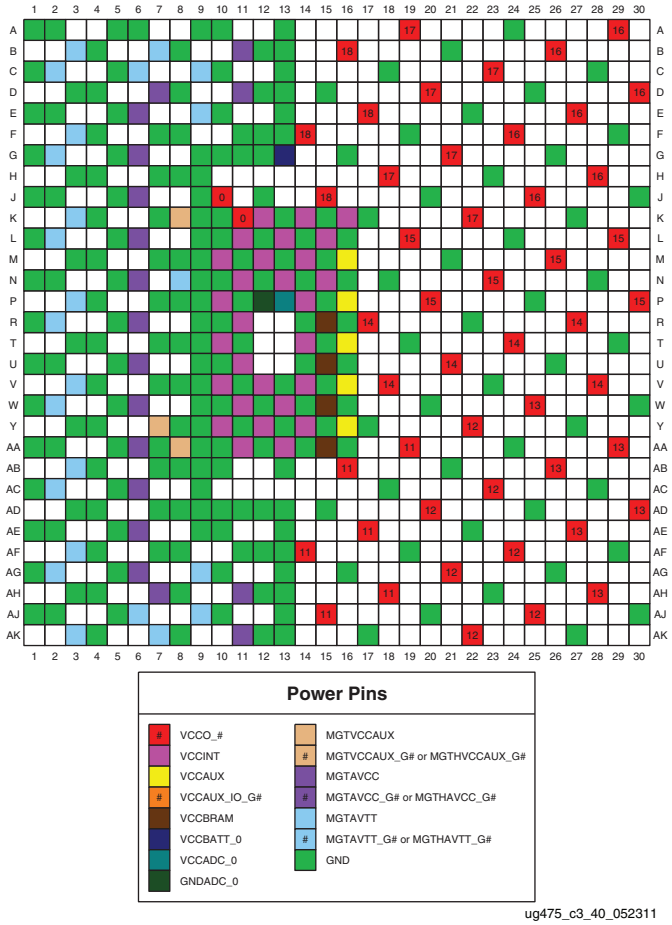
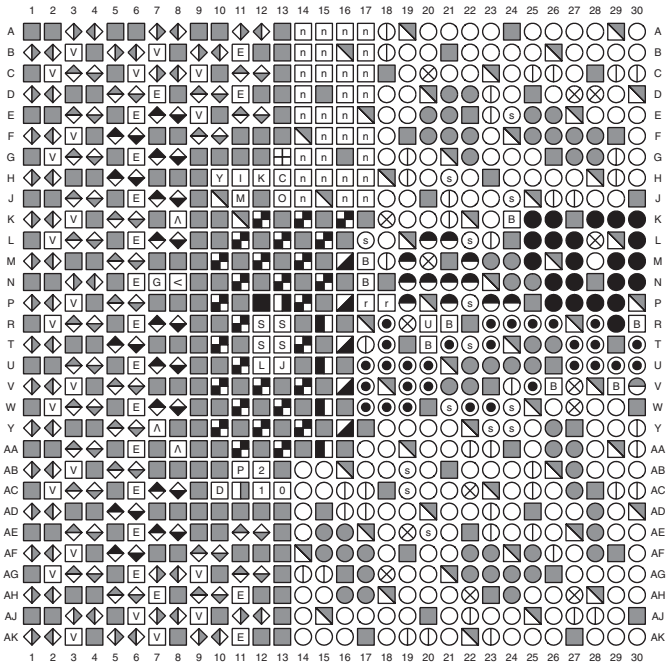


Figure 3-36: **FFG901 Package—XC7K355T Power and GND Placement**

www.BDTIC.com/XILINX

FFG901 Package—XC7K420T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_#	MGTAVCC_G#	CCLK_0	VP_0	GND
IO_XX_#	MGTAVTT_G#	CFGBVS_0	VN_0	VCCAUX_IO_G#
Multi–Function Pins	MGTVCCAUX_G#	DONE_0	VREFP_0	VCCAUX
ADV_B	VRN	MGTAVTTRCAL	DXP_0	VREFN_0	VCCINT
FCS_B	VRP	MGTRREF	DXN_0	VCCO_#
FOE_B	VREF	MGTREFCLK1/0P	GNDADC_0	VCCBRAM
MOSI	D00–D31	MGTREFCLK1/0N	INIT_B_0	NC
FWE_B	A00–A28	MGTXRXP	M0_0
DOUT_CSO_B	DQS	MGTXRXN	M1_0
CSI_B	MRCC	MGTXTXP	M2_0
PUDC_B	SRCC	MGTXTXN	PROGRAM_B_0
RDWR_B	MGTHAVCC_G#	TCK_0
RS0–RS1	MGTHAVTT_G#	TDI_0
AD0P/AD0N–AD15P/AD15N	MGTHRXP	TDO_0
EMCCLK	MGTHRXN	TMS_0
	MGTHTXP	VCCADC_0
	MGTHTXN	VCCBATT_0

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Figure 3-37: **FFG901 Package—XC7K420T Pinout Diagram**

www.BDTIC.com/XILINX

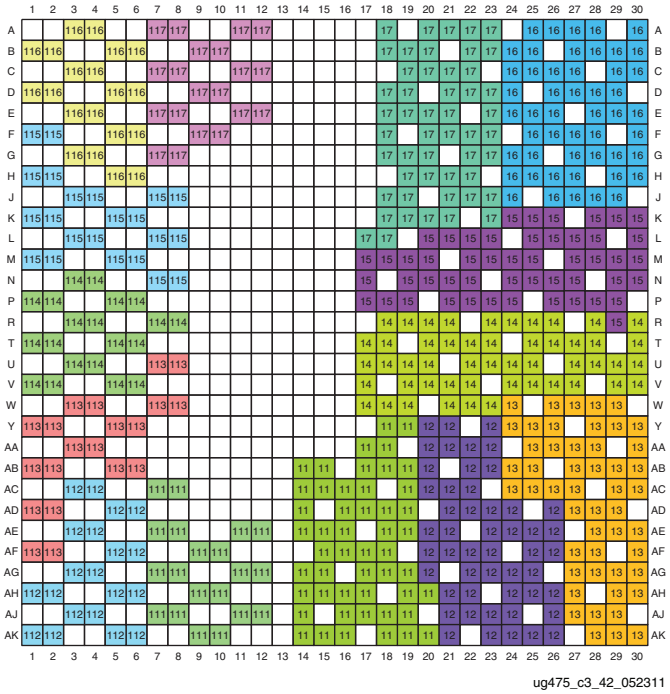

Figure 3-38: **FFG901 Package—XC7K420T I/O Banks**

www.BDTIC.com/XILINX

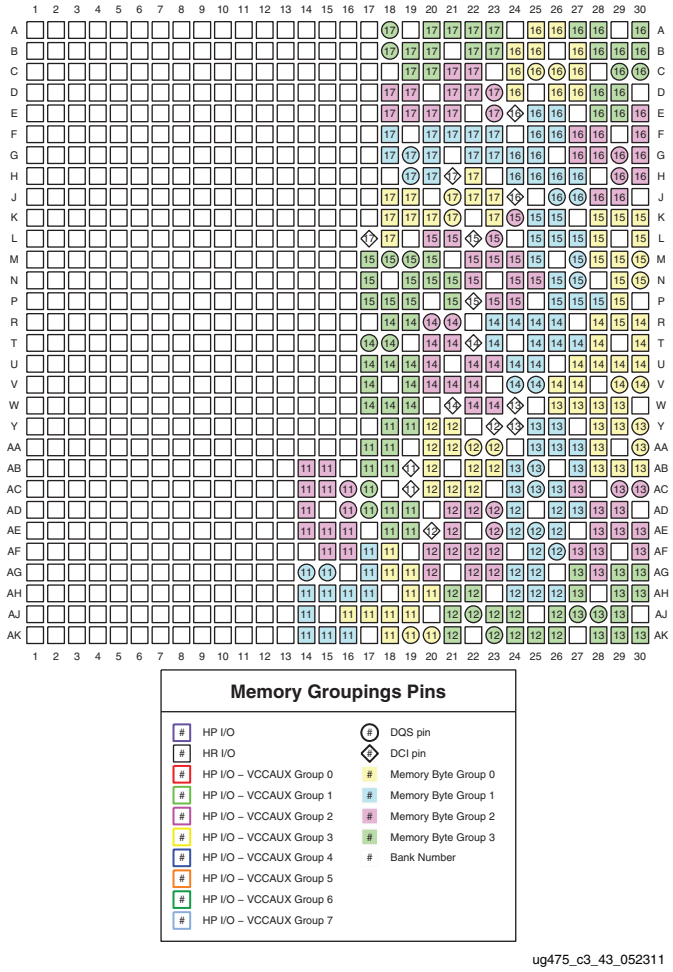

Figure 3-39: **FFG901 Package—XC7K420T Memory Groupings**

www.BDTIC.com/XILINX

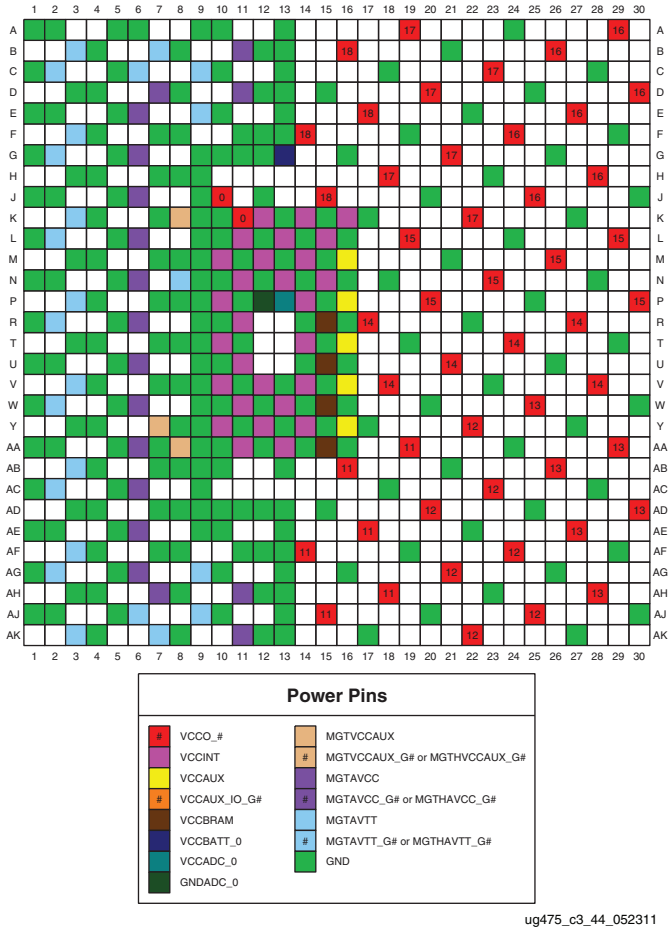

Figure 3-40: **FFG901 Package—XC7K420T Power and GND Placement**

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FFG901 Package—XC7K480T

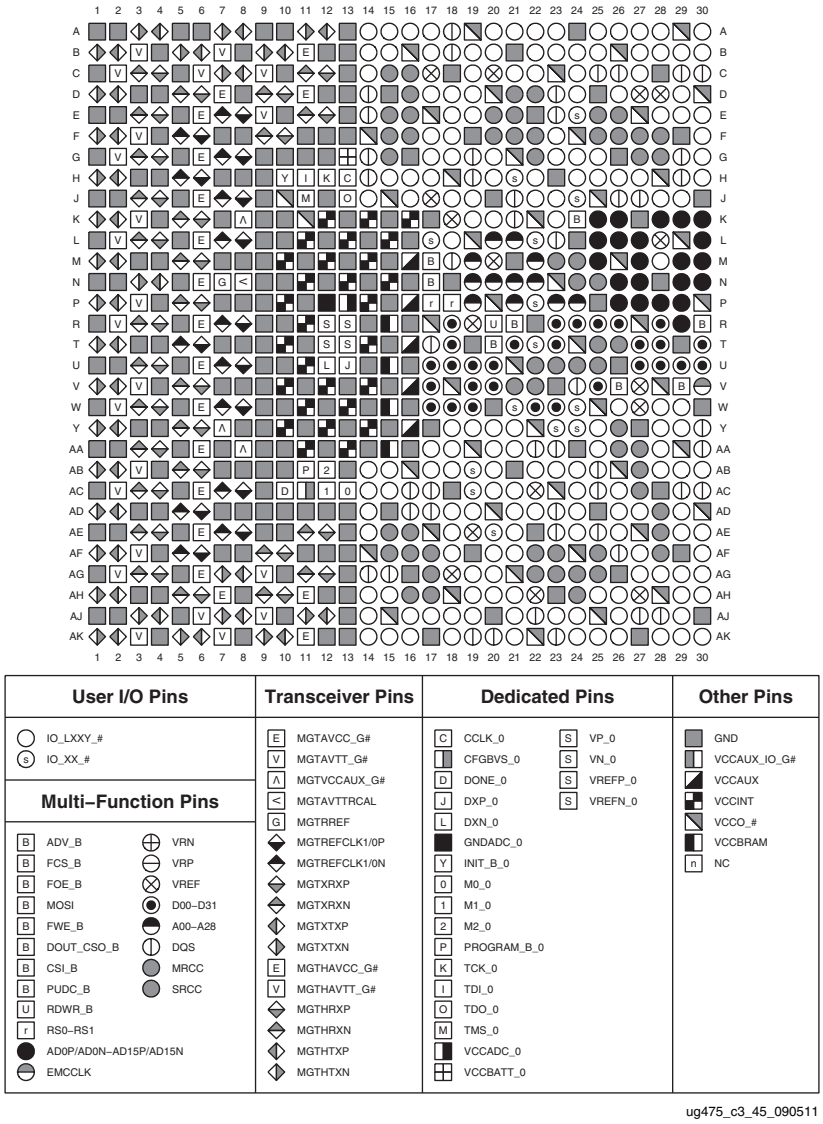

Figure 3-41: **FFG901 Package—XC7K480T Pinout Diagram**

www.BDTIC.com/XILINX

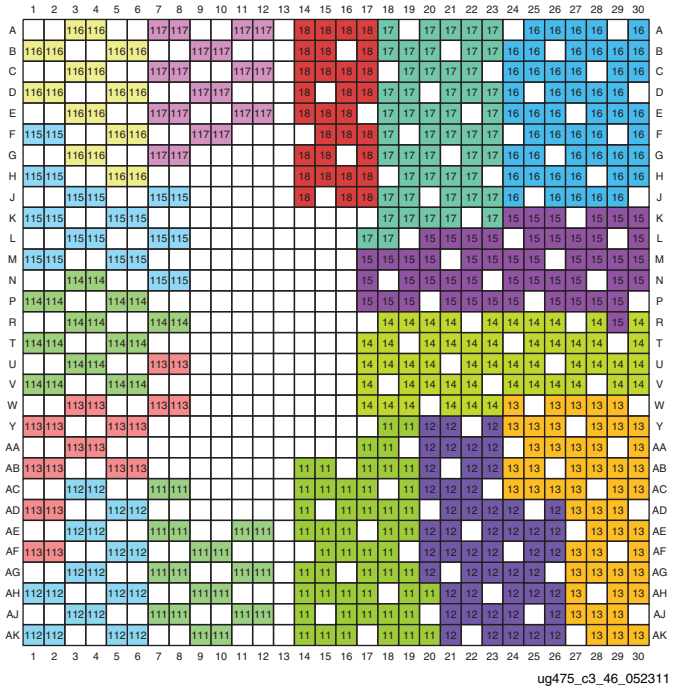

Figure 3-42: **FFG901 Package—XC7K480T I/O Banks**

www.BDTIC.com/XILINX

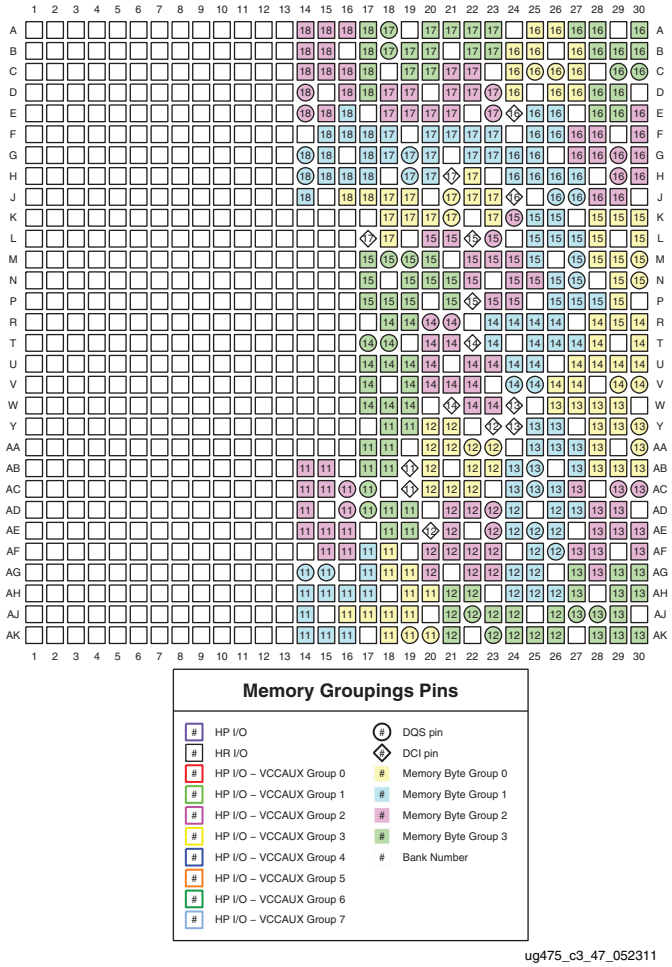

Figure 3-43: **FFG901 Package—XC7K480T Memory Groupings**

www.BDTIC.com/XILINX

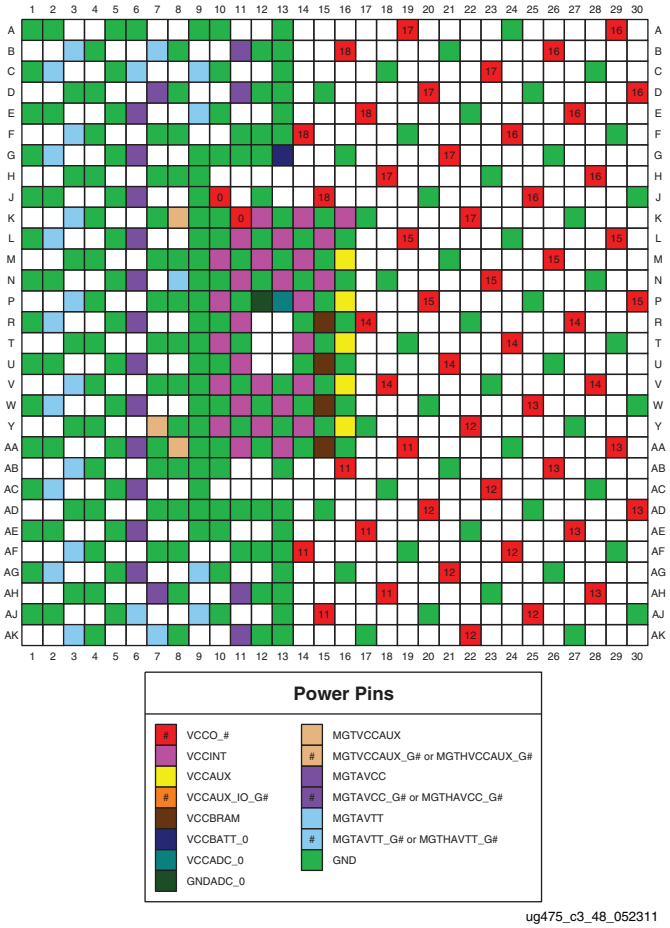

Figure 3-44: **FFG901 Package—XC7K480T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1156 Package—XC7K420T

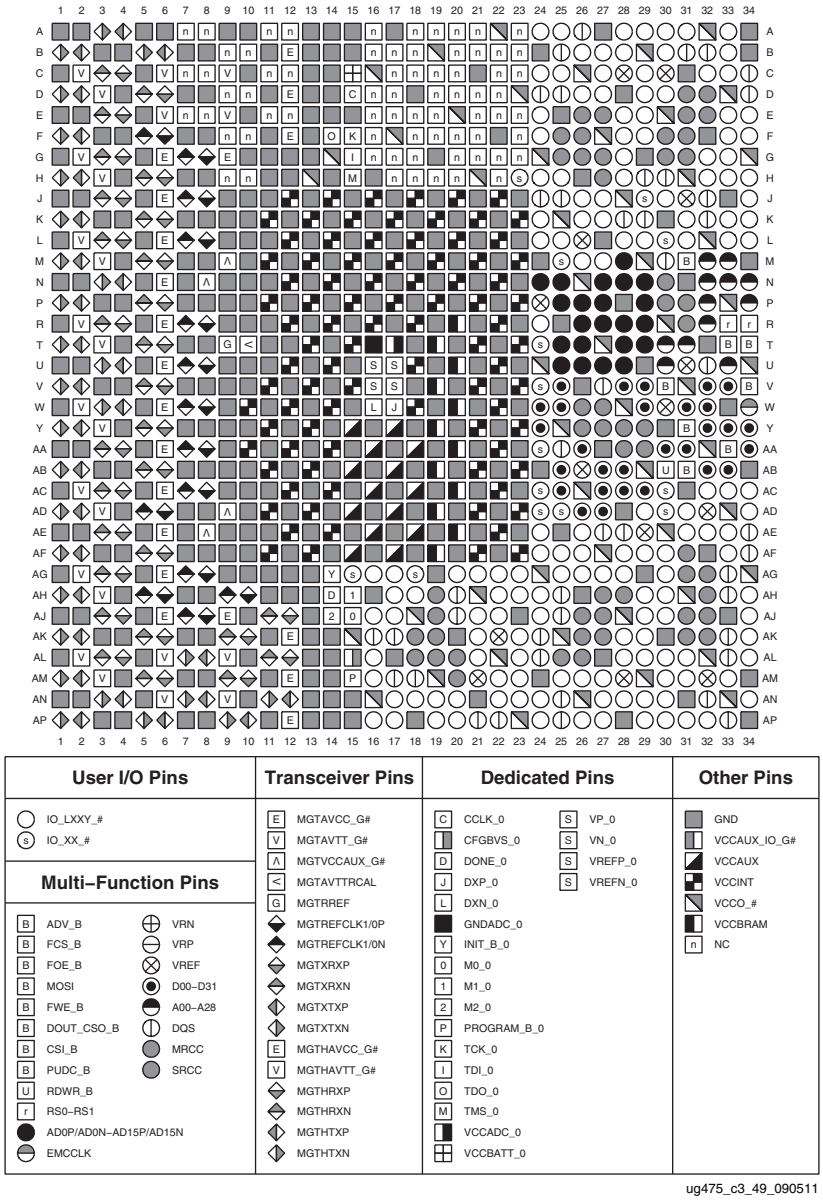

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Figure 3-45: **FFG1156 Package—XC7K420T Pinout Diagram**

www.BDTIC.com/XILINX

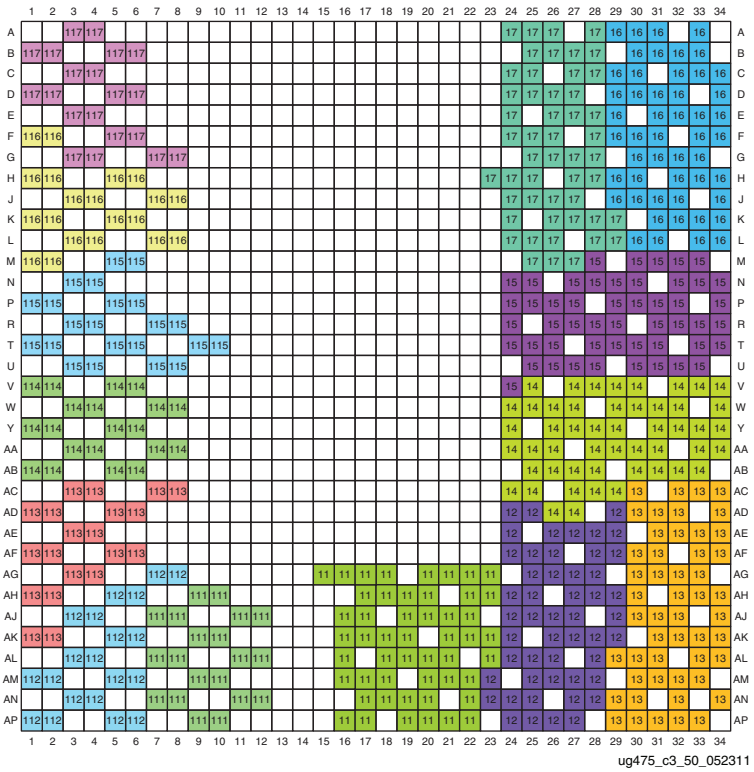

Figure 3-46: **FFG1156 Package—XC7K420T I/O Banks**

www.BDTIC.com/XILINX
www.xilinx.com

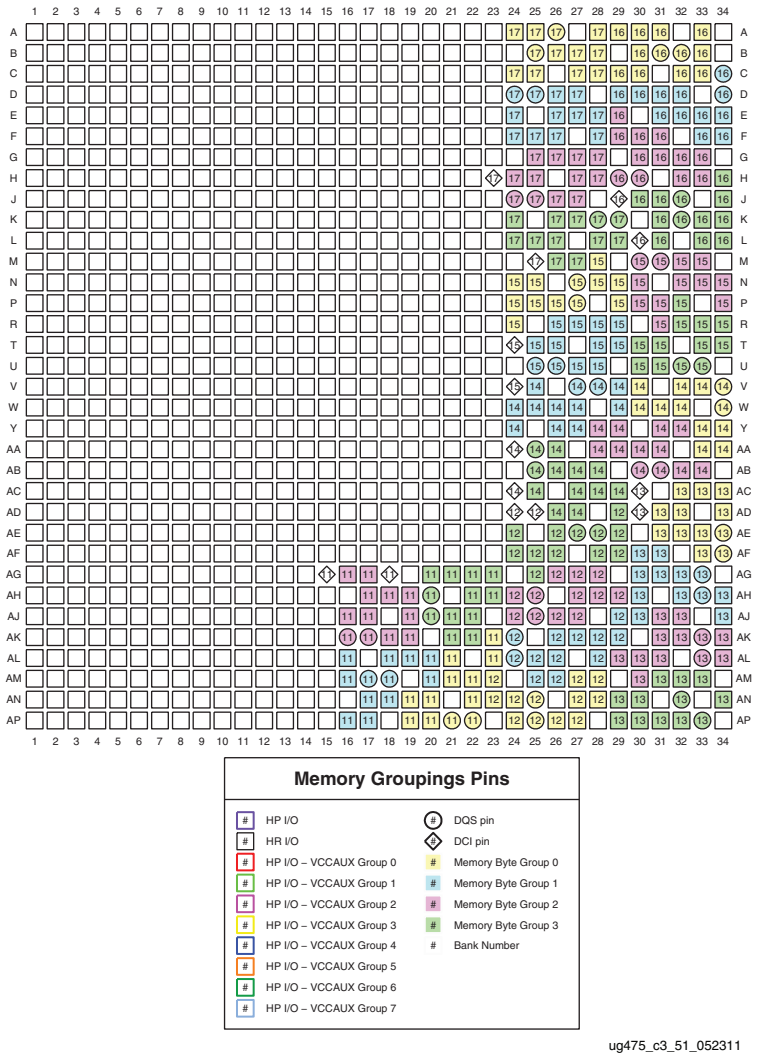

Figure 3-47: **FFG1156 Package—XC7K420T Memory Groupings**

www.BDTIC.com/XILINX

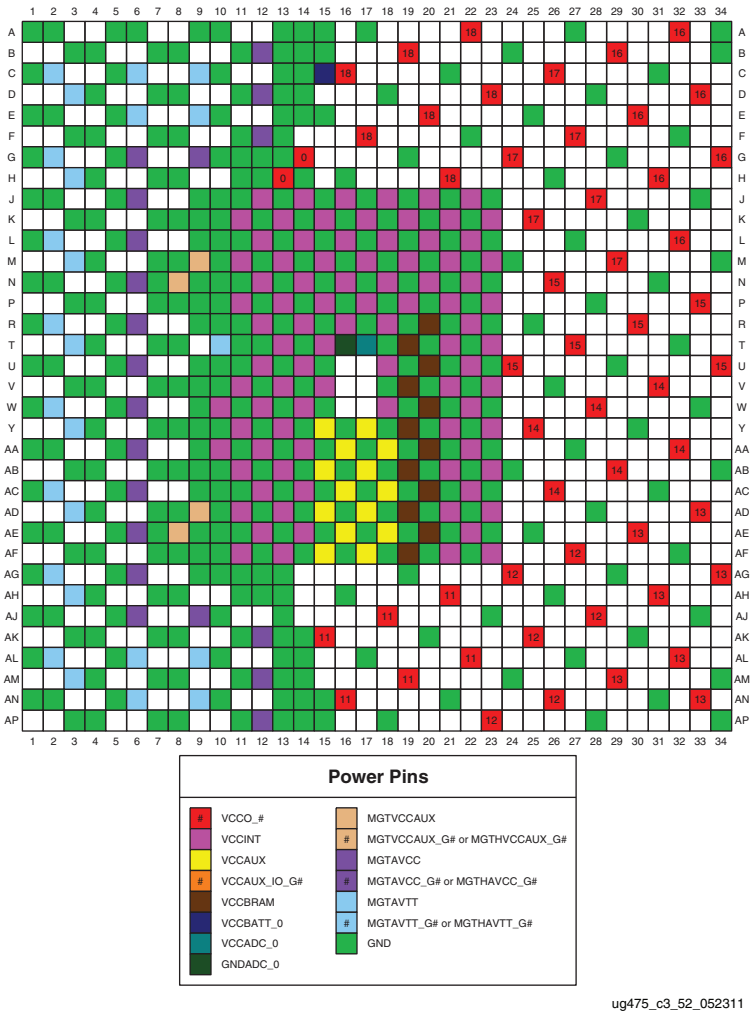

Figure 3-48: **FFG1156 Package—XC7K420T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1156 Package—XC7K480T

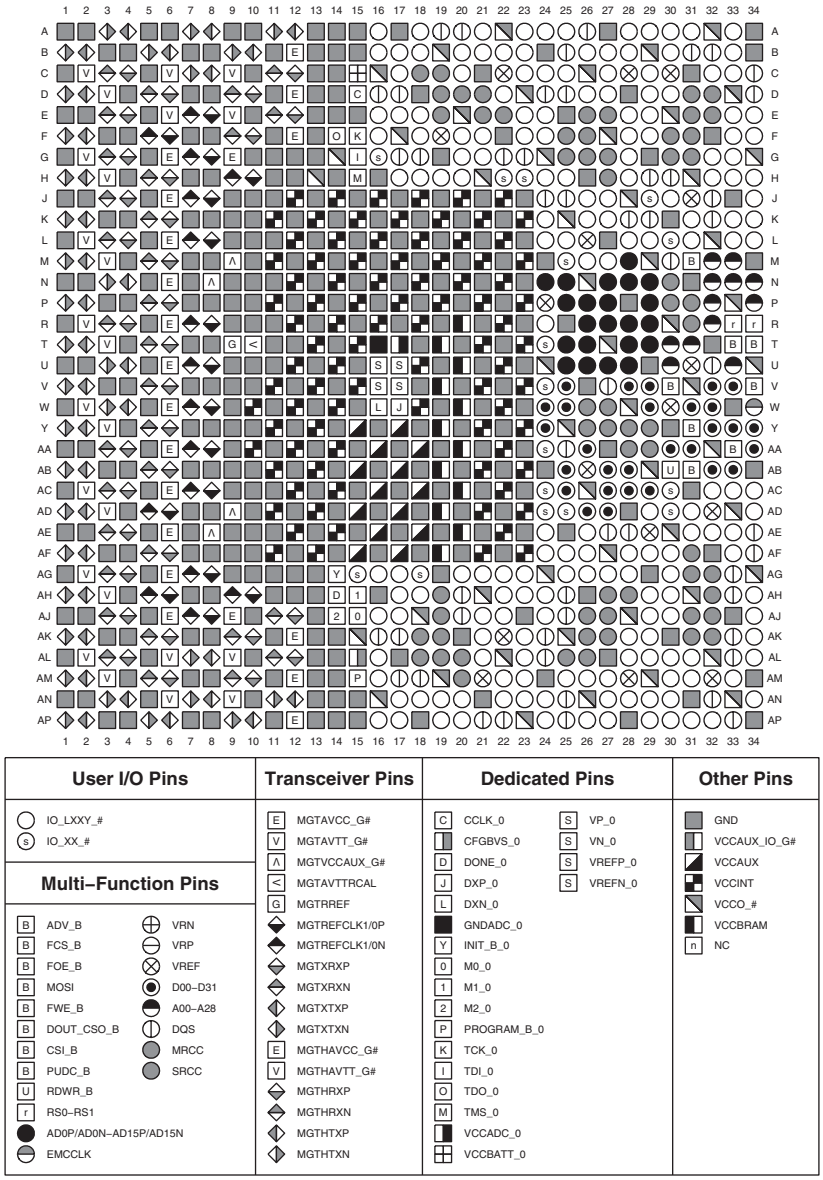

Figure 3-49: **FFG1156 Package—XC7K480T Pinout Diagram**

www.BDTIC.com/XILINX

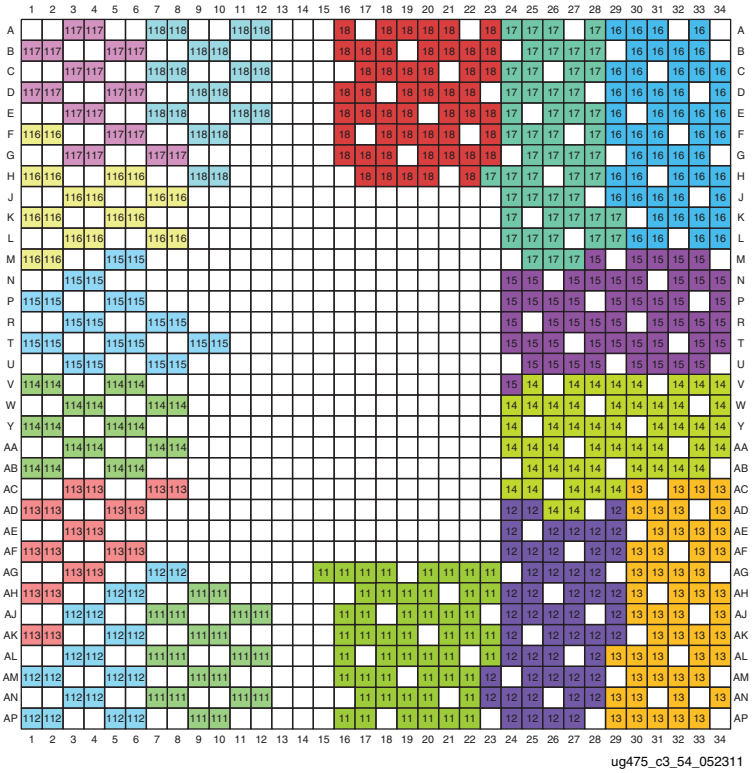

Figure 3-50: **FFG1156 Package—XC7K480T I/O Banks**

www.BDTIC.com/XILINX

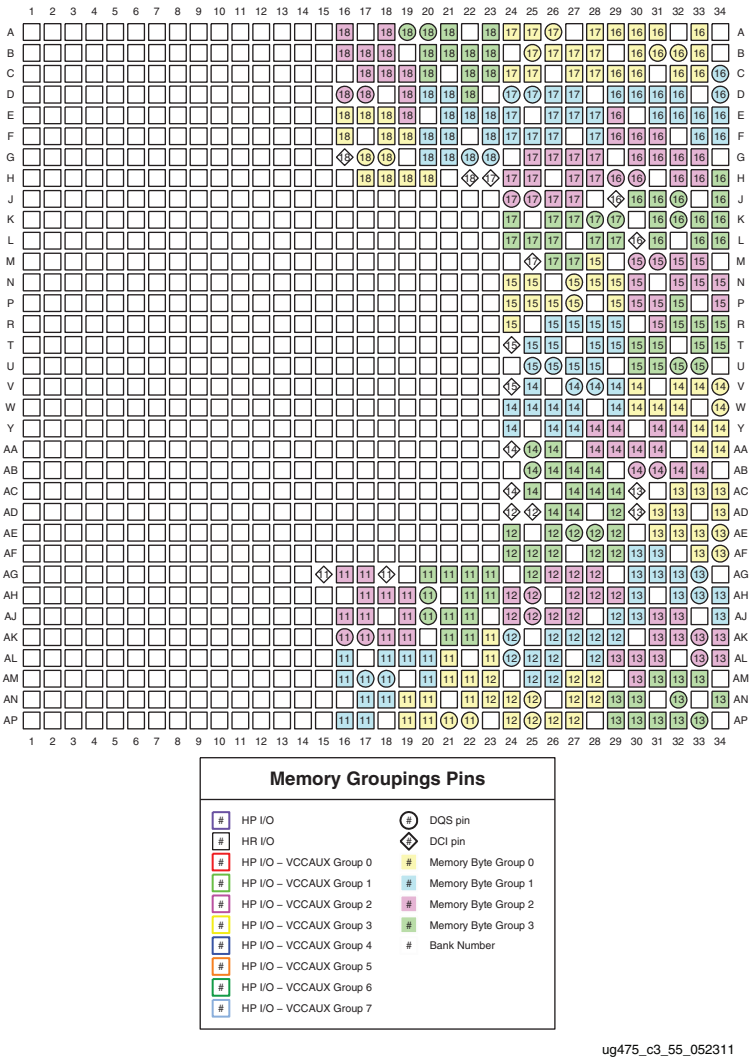

Figure 3-51: **FFG1156 Package—XC7K480T Memory Groupings**

www.BDTIC.com/XILINX

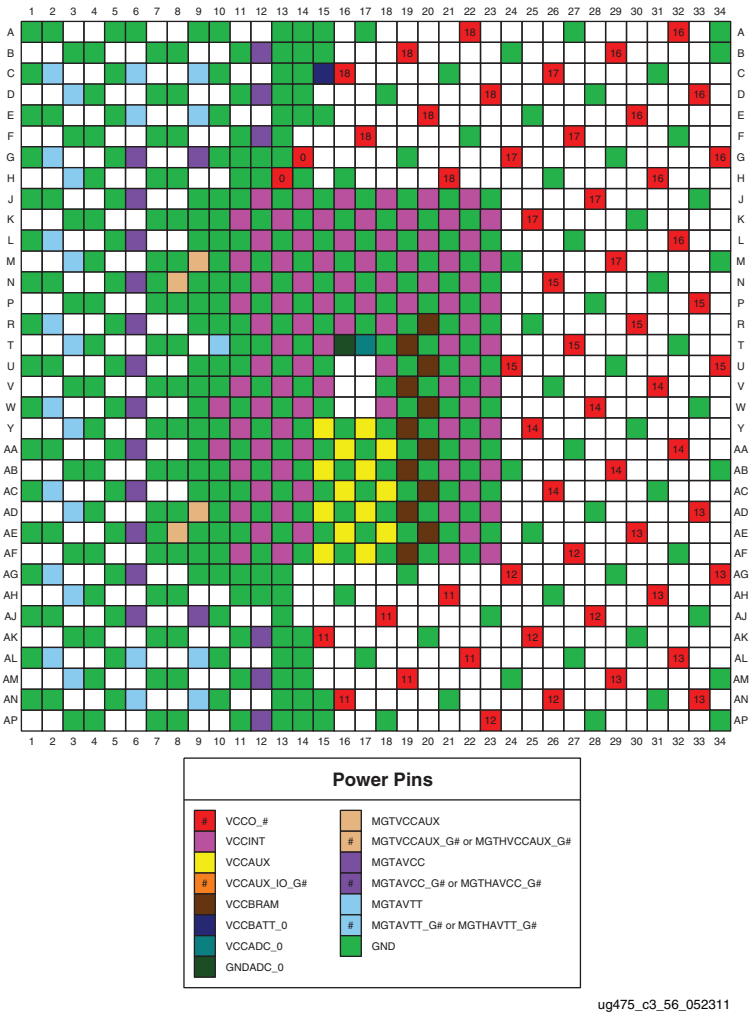

Figure 3-52: **FFG1156 Package—XC7K480T Power and GND Placement**

www.BDTIC.com/XILINX

Virtex-7 FPGAs Device Diagrams

Table 3-3: **Virtex-7 FPGAs Device Diagrams Cross Reference**

Device	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FF(G)	FL(G)	FL(G)	FL(G)	FL(G)	FH(G)
	1157	1158	1761	1926	1927	1928	1930	1761	1925	1928	1930	1761
XC7V585T	page 98		page 102									
XC7V1500T								FL1761/ FLG1761				
XC7V2000T									page 106			page 110
XC7VX330T	FF1157/ FFG1157		FF1761/ FFG1761									
XC7VX415T	FF1157/ FFG1157	FF1158/ FFG1158			FF1927/ FFG1927							
XC7VX485T	page 114	page 118	page 122		page 126		page 130					
XC7VX550T		FF1158/ FFG1158			FF1927/ FFG1927							
XC7VX690T	FF1157/ FFG1157	FF1158/ FFG1158	FF1761/ FFG1761	FF1926/ FFG1926	FF1927/ FFG1927		FF1930/ FFG1930					
XC7VX980T				FF1926/ FFG1926		FF1928/ FFG1928	FF1930/ FFG1930					
XC7VX1140T										FL1928/ FLG1928	FL1930/ FLG1930	

Note: The available files are listed in Table 3-3 are linked. Figures for some Virtex-7 FPGAs are in development.

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FFG1157 Package—XC7V585T

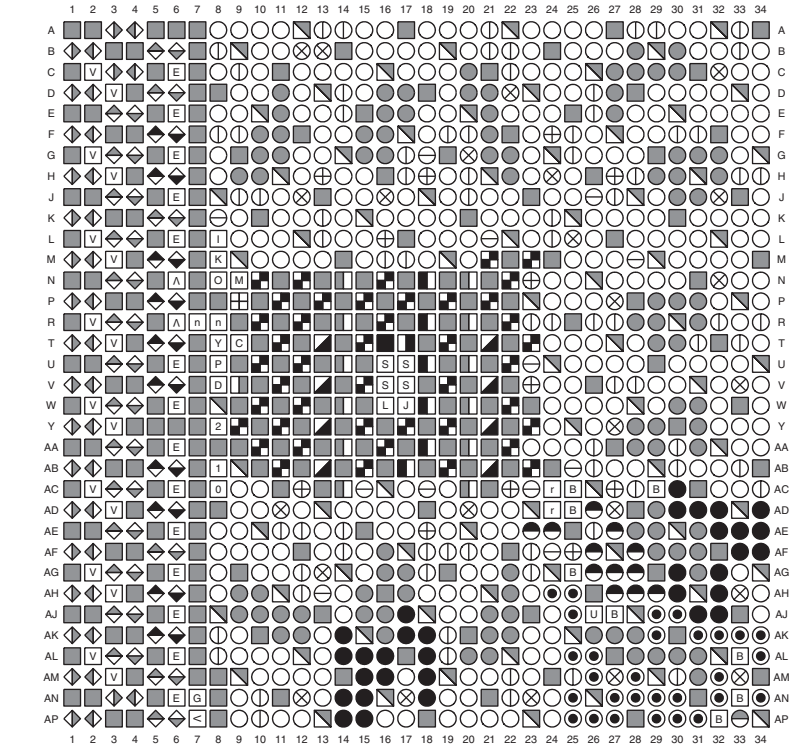


Figure 3-53: **FF(G)1157 Package—XC7V585T Pinout Diagram**

www.BDTIC.com/XILINX

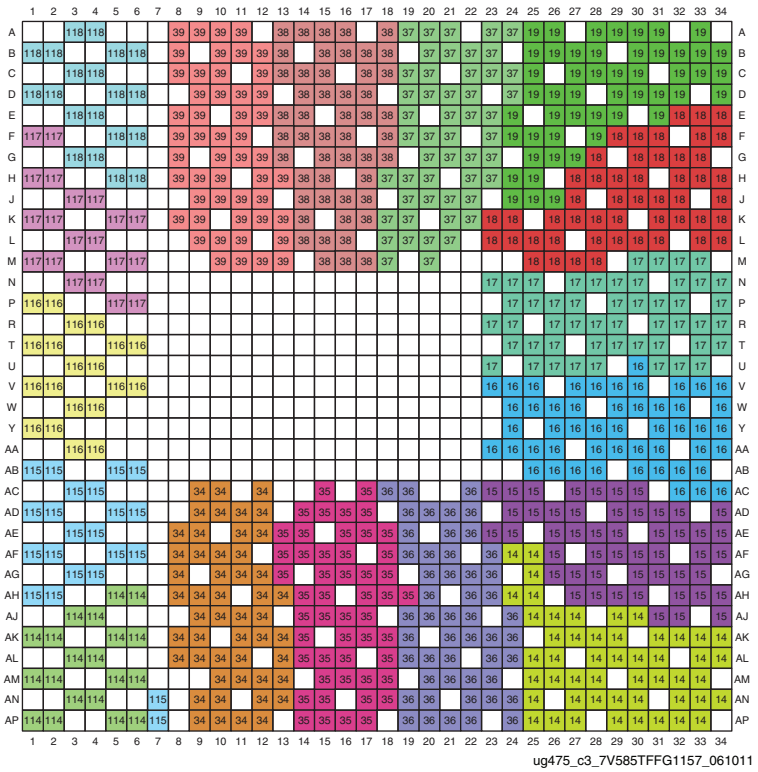


Figure 3-54: **FF(G)1157 Package—XC7V585T I/O Banks**

www.BDTIC.com/XILINX

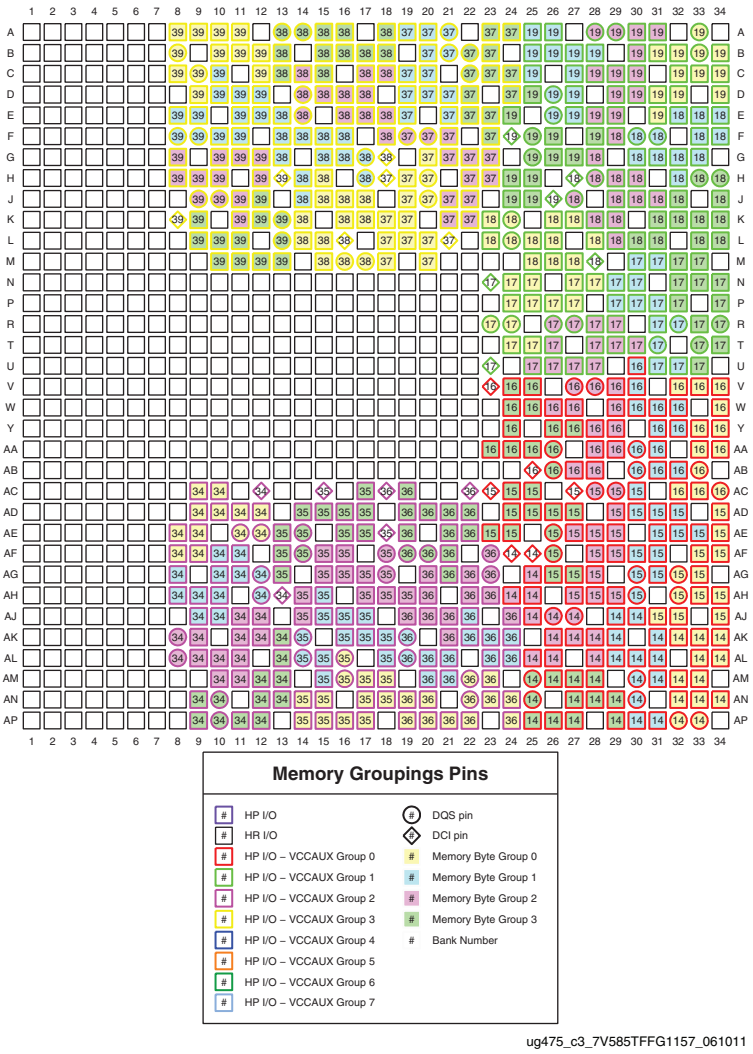


Figure 3-55: **FF(G)1157 Package—XC7V585T Memory Groupings**

www.BDTIC.com/XILINX

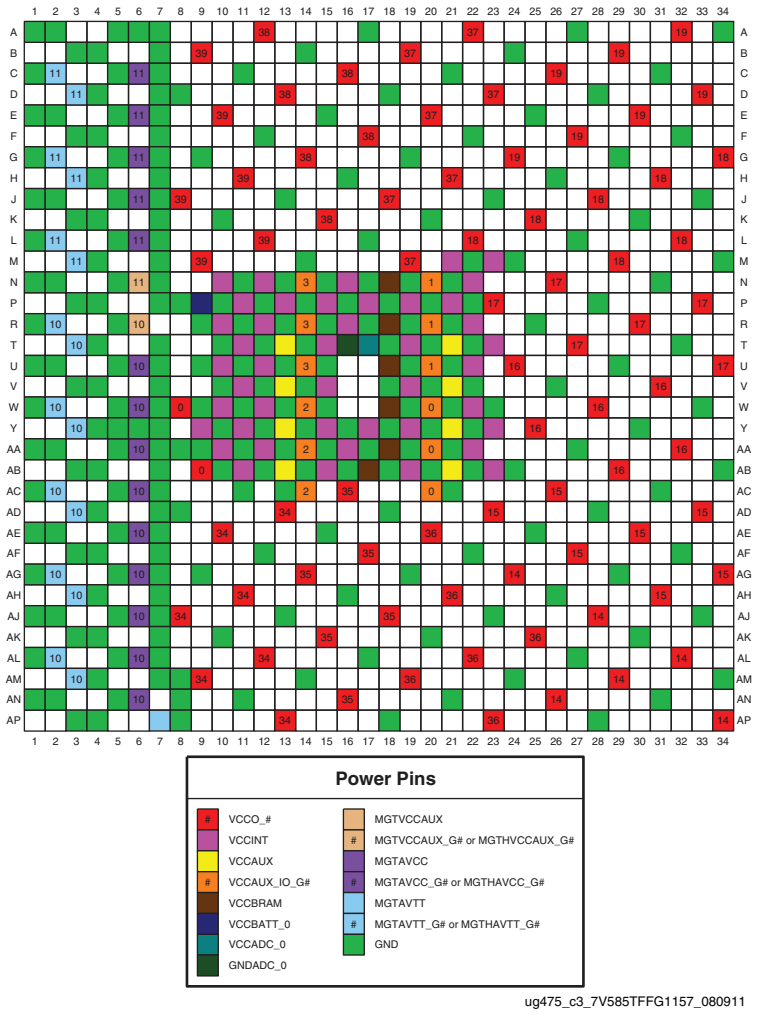


Figure 3-56: **FF(G)1157 Package—XC7V585T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1761 Package—XC7V585T

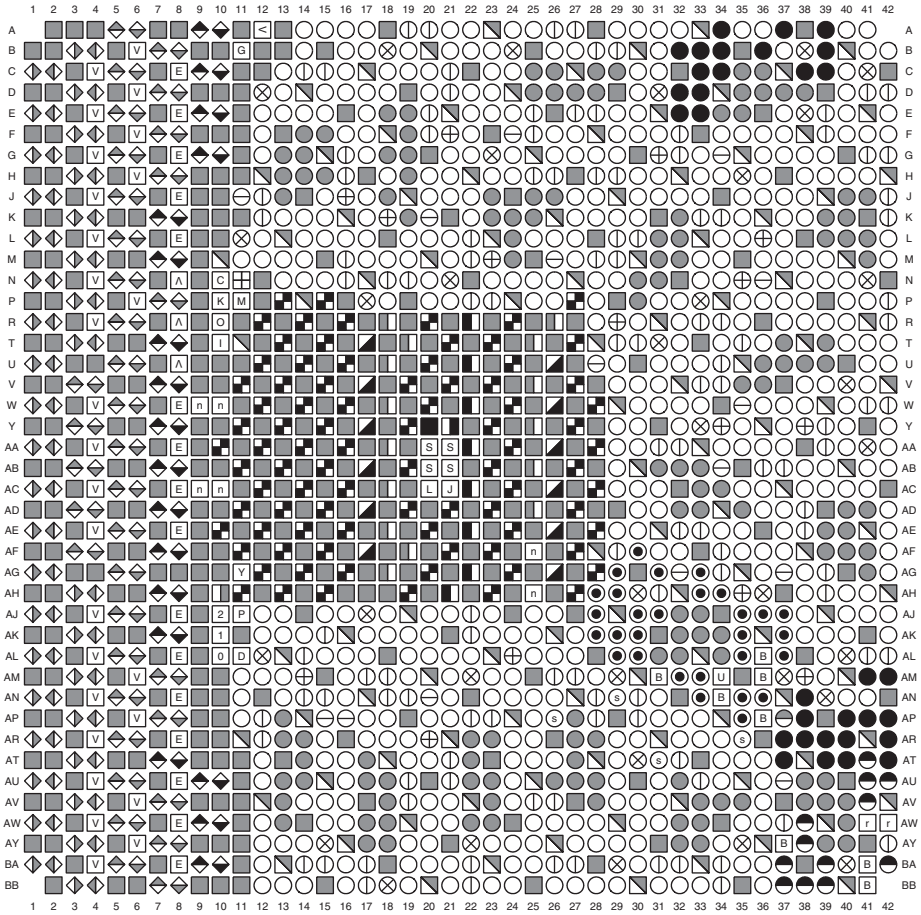


Figure 3-57: **FF(G)1761 Package—XC7V585T Pinout Diagram**

www.BDTIC.com/XILINX

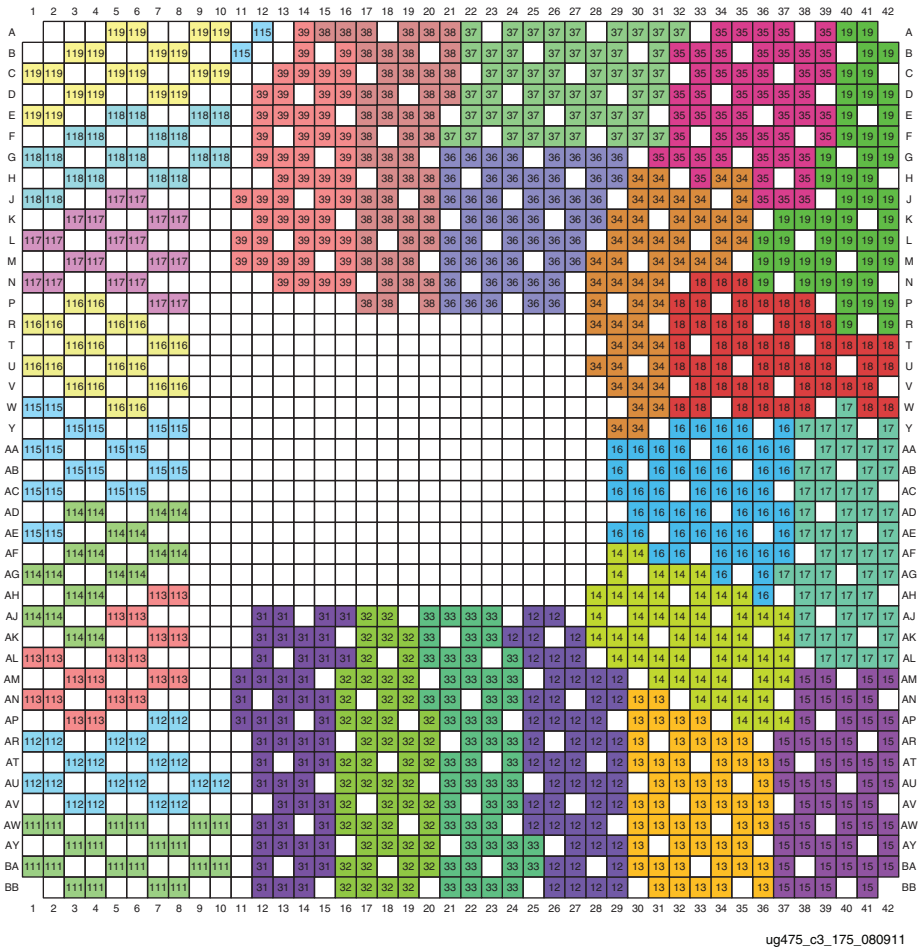


Figure 3-58: **FF(G)1761 Package—XC7V585T I/O Banks**

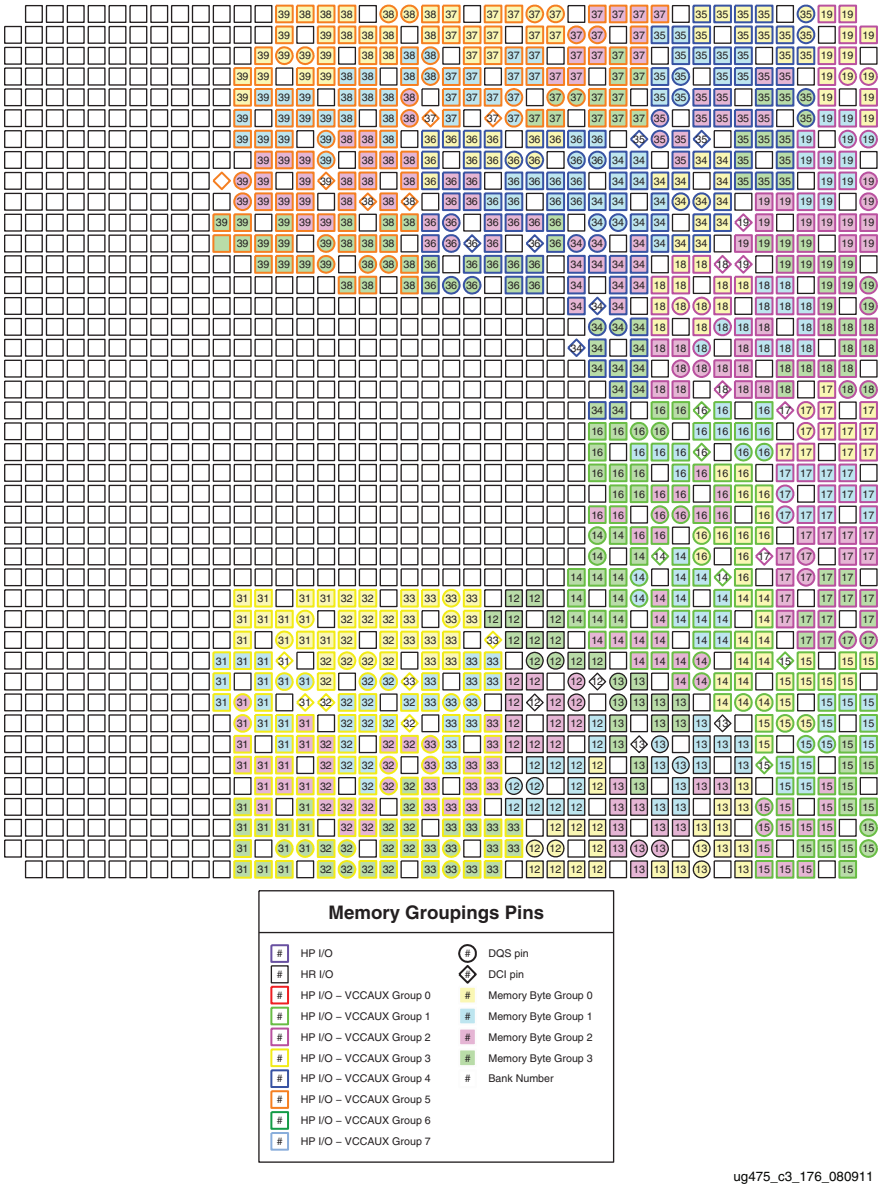


Figure 3-59: **FF(G)1761 Package—XC7V585T Memory Groupings**

www.BDTIC.com/XILINX
www.xilinx.com

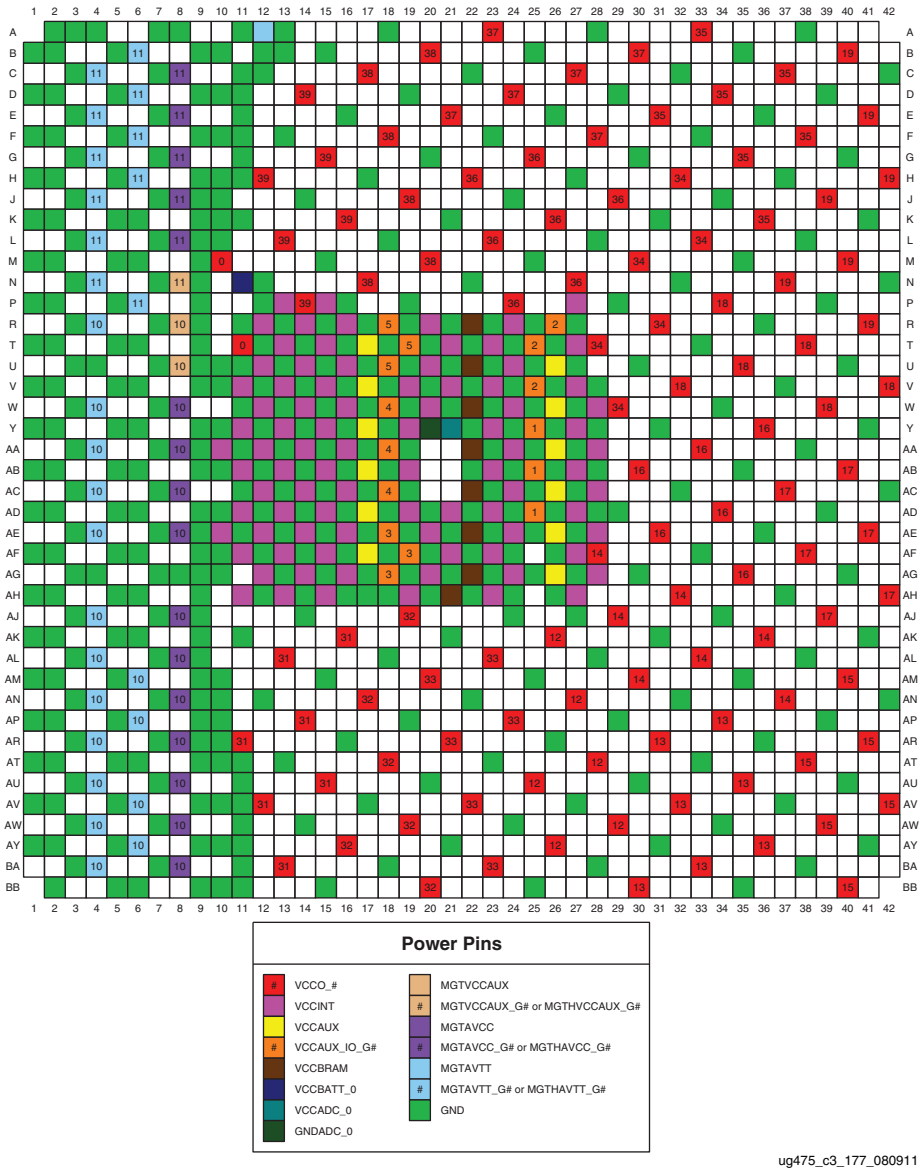
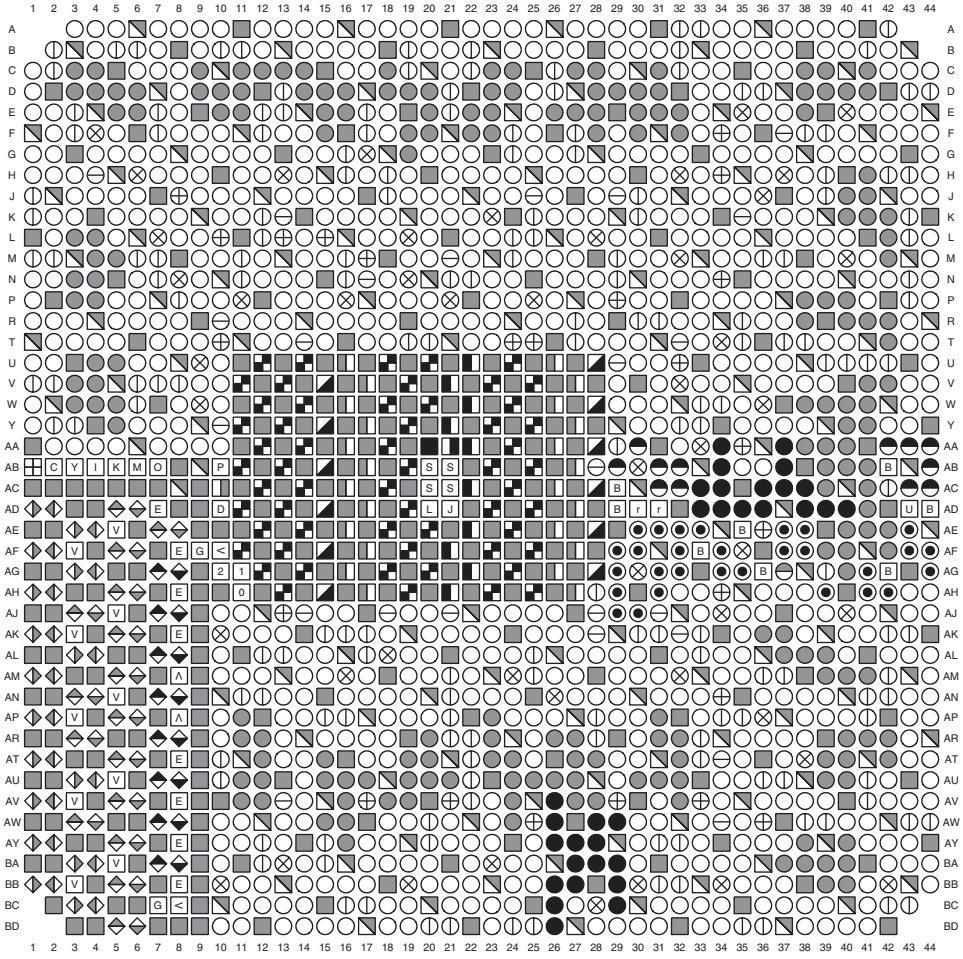


Figure 3-60: **FF(G)1761 Package—XC7V585T Power and GND Placement**

www.BDTIC.com/XILINX

FLG1925 Package—XC7V2000T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_# IO_XX_#	MGTAVCC_G# MGTAVTT_G# MGTVCCAUX_G# MGTAVTTRCAL MGTRREF MGTREFCLK1/0P MGTREFCLK1/0N MGTXRXP MGTXRXN MGTXTXP MGTXTXN MGTHAVCC_G# MGTHAVTT_G# MGTHRXP MGTHRXN MGTHTXP MGTHTXN	CCLK_0 CFGBVS_0 DONE_0 DXP_0 DXN_0 GNDADC_0 INIT_B_0 M0_0 M1_0 M2_0 PROGRAM_B_0 TCK_0 TDI_0 TDO_0 TMS_0 VCCADC_0 VCCBATT_0 VP_0 VN_0 VREFP_0 VREFN_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC

Multi–Function Pins

ADV_B, FCS_B, FOE_B, MOSI, FWE_B, DOUT_CSO_B, CSI_B, PUDC_B, RDWR_B, RS0–RS1, AD0P/AD0N–AD15P/AD15N, EMCCLK, VRN, VRP, VREF, D00–D31, A00–A28, DQS, MRCC, SRCC

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Figure 3-61: **FLG1925 Package—XC7V2000T Pinout Diagram**

www.BDTIC.com/XILINX

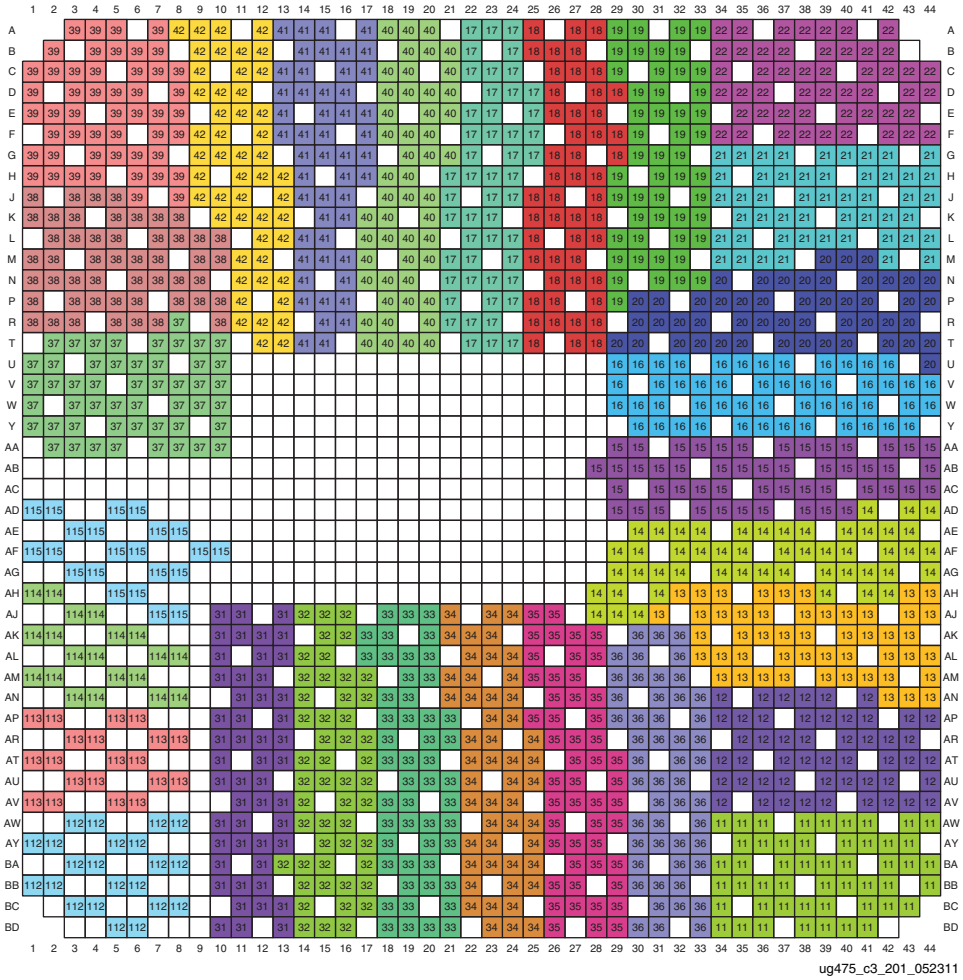


Figure 3-62: **FLG1925 Package—XC7V2000T I/O Banks**

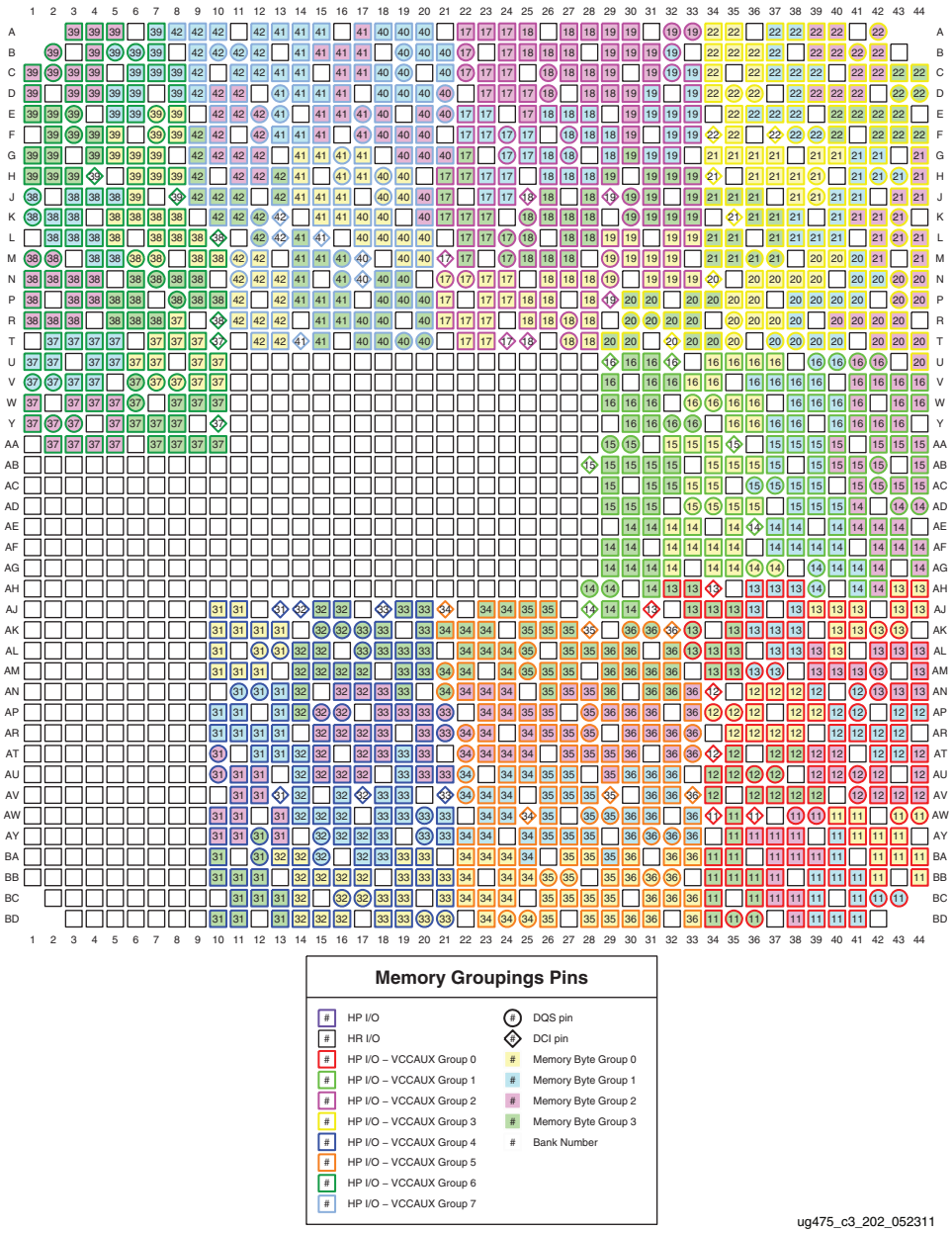


Figure 3-63: **FLG1925 Package—XC7V2000T Memory Groupings**

www.BDTIC.com/XILINX

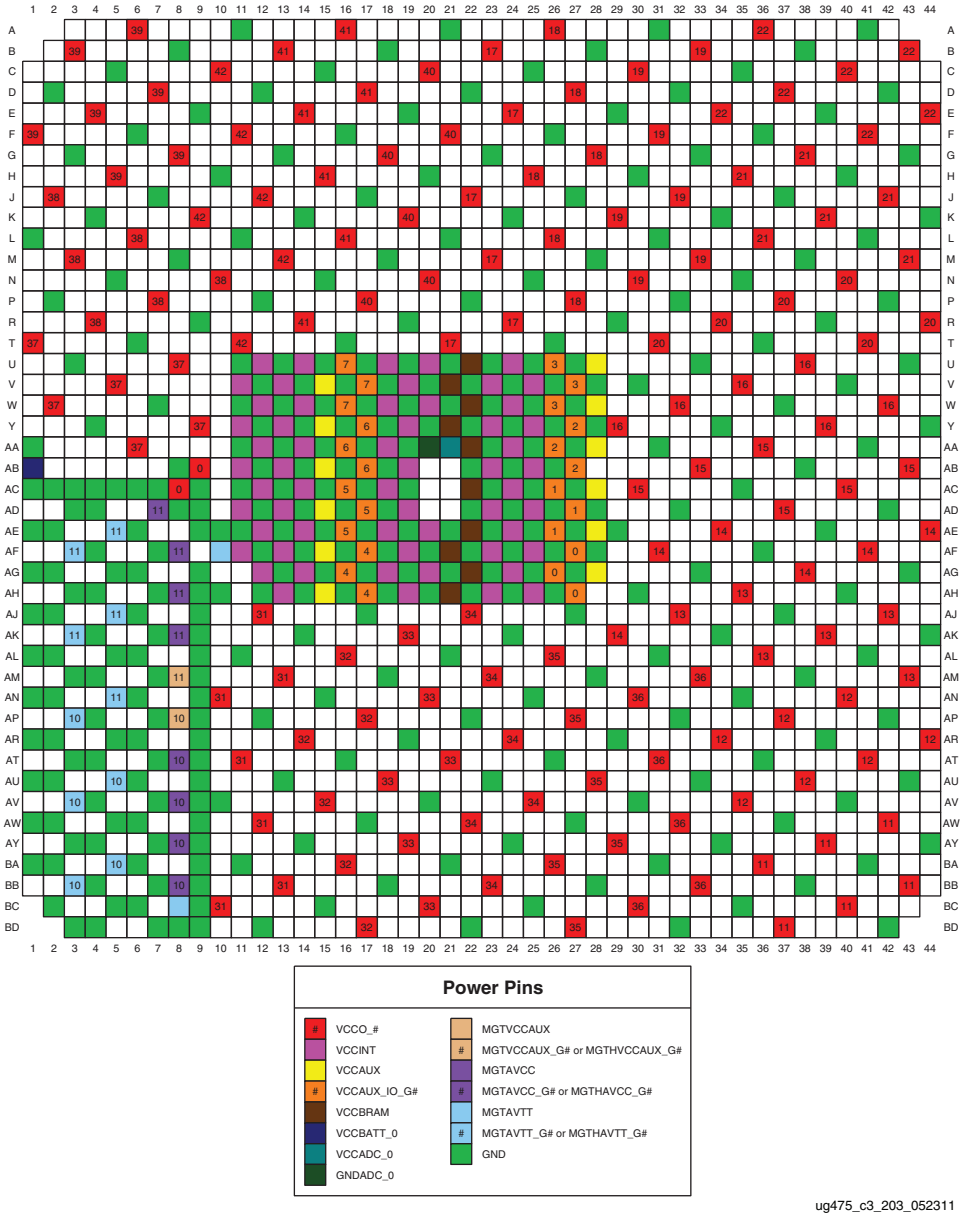


Figure 3-64: **FLG1925 Package—XC7V2000T Power and GND Placement**

www.BDTIC.com/XILINX

FHG1761 Package—XC7V2000T

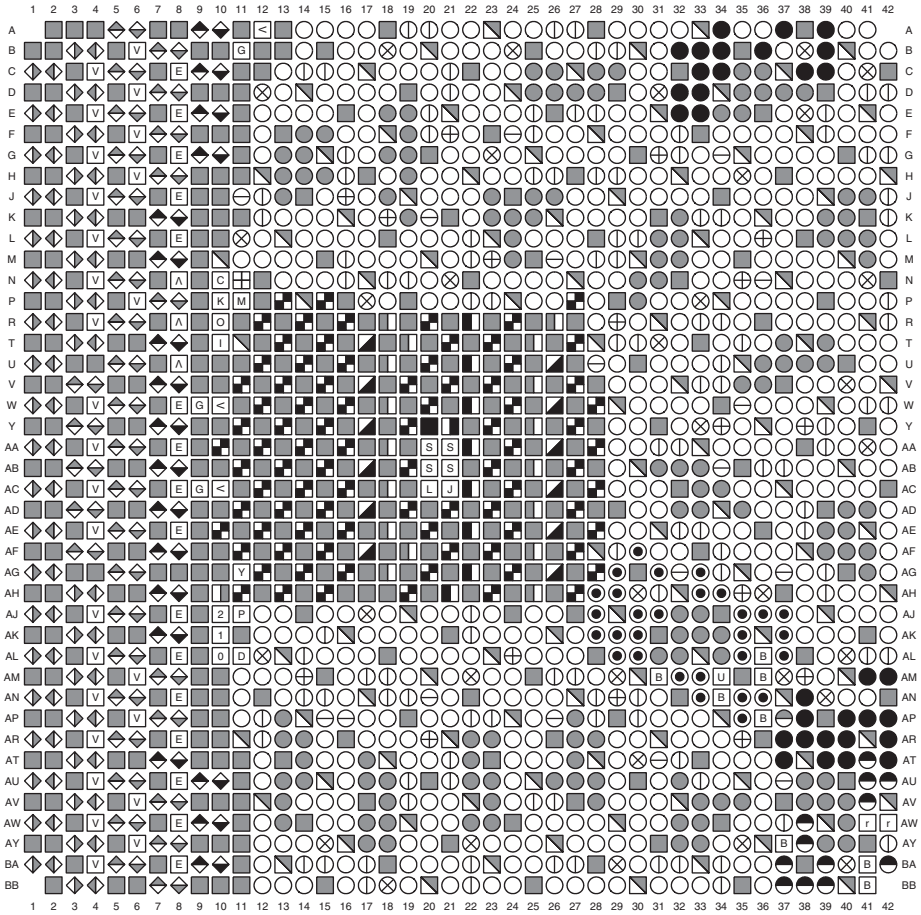


Figure 3-65: **FHG1761 Package—XC7V2000T Pinout Diagram**

www.BDTIC.com/XILINX

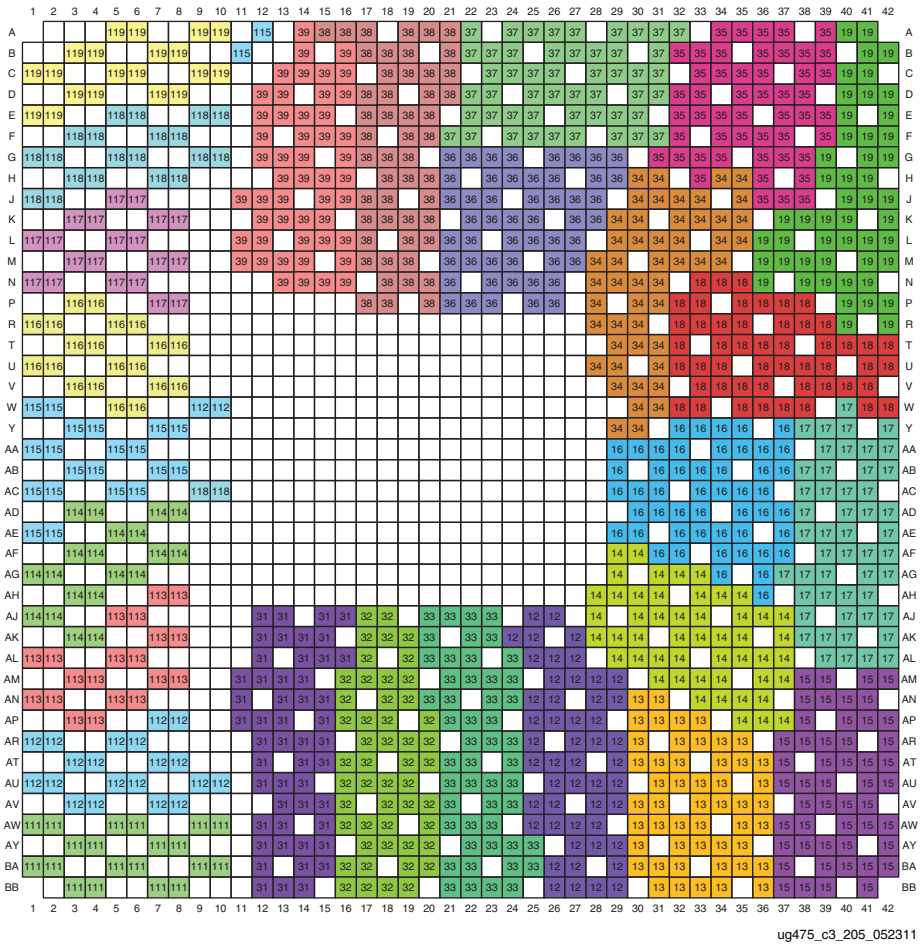


Figure 3-66: **FHG1761 Package—XC7V2000T I/O Banks**

www.BDTIC.com/XILINX

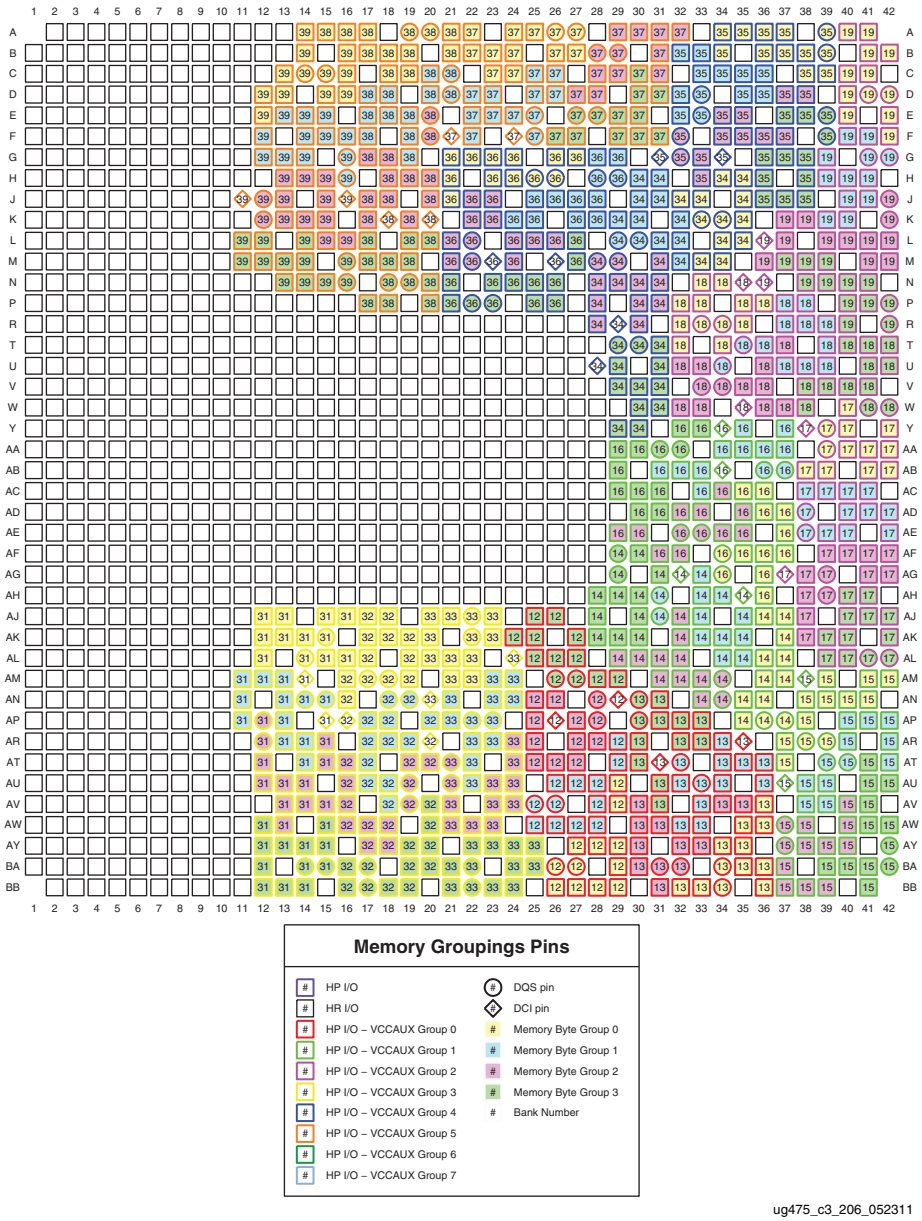


Figure 3-67: **FHG1761 Package—XC7V2000T Memory Groupings**

www.BDTIC.com/XILINX

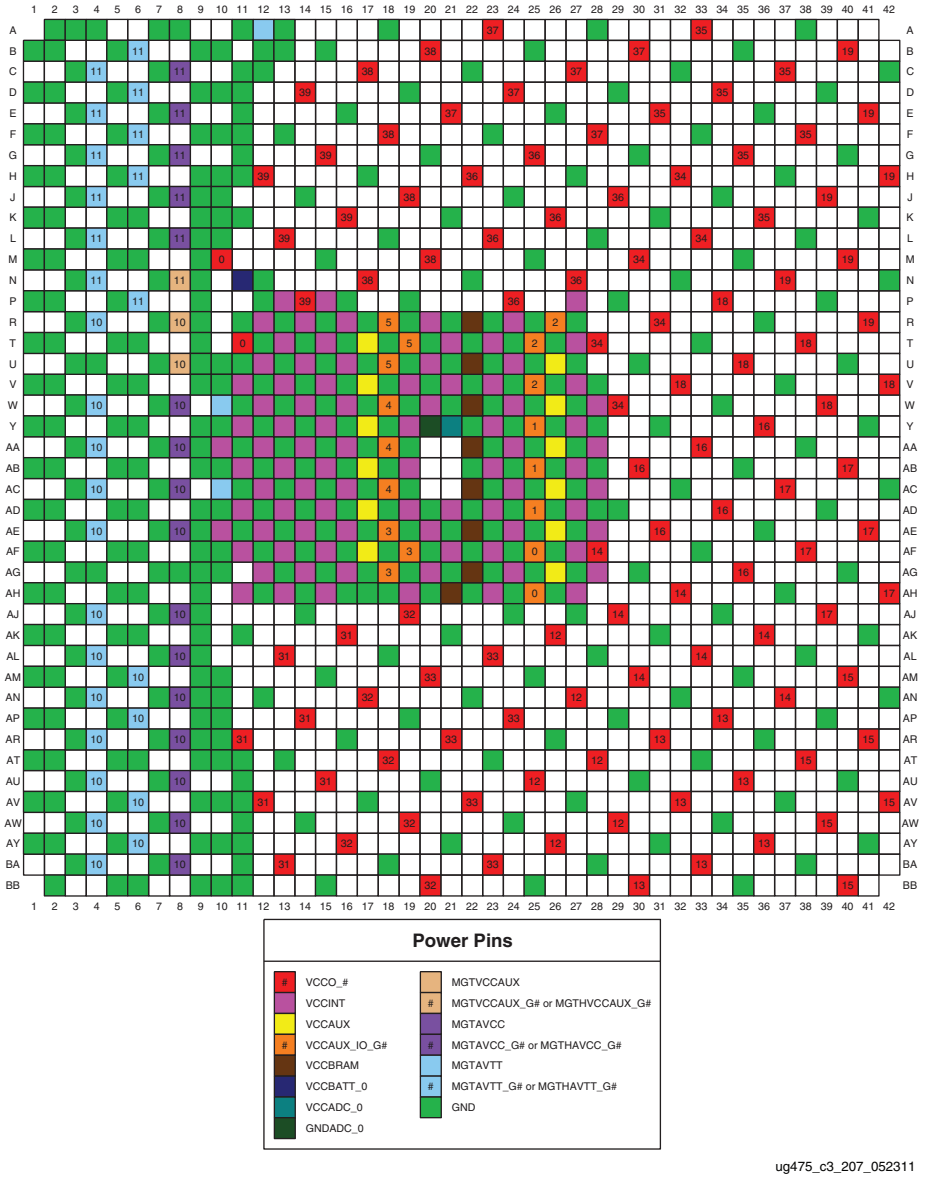


Figure 3-68: **FHG1761 Package—XC7V2000T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1157 Package—XC7VX485T

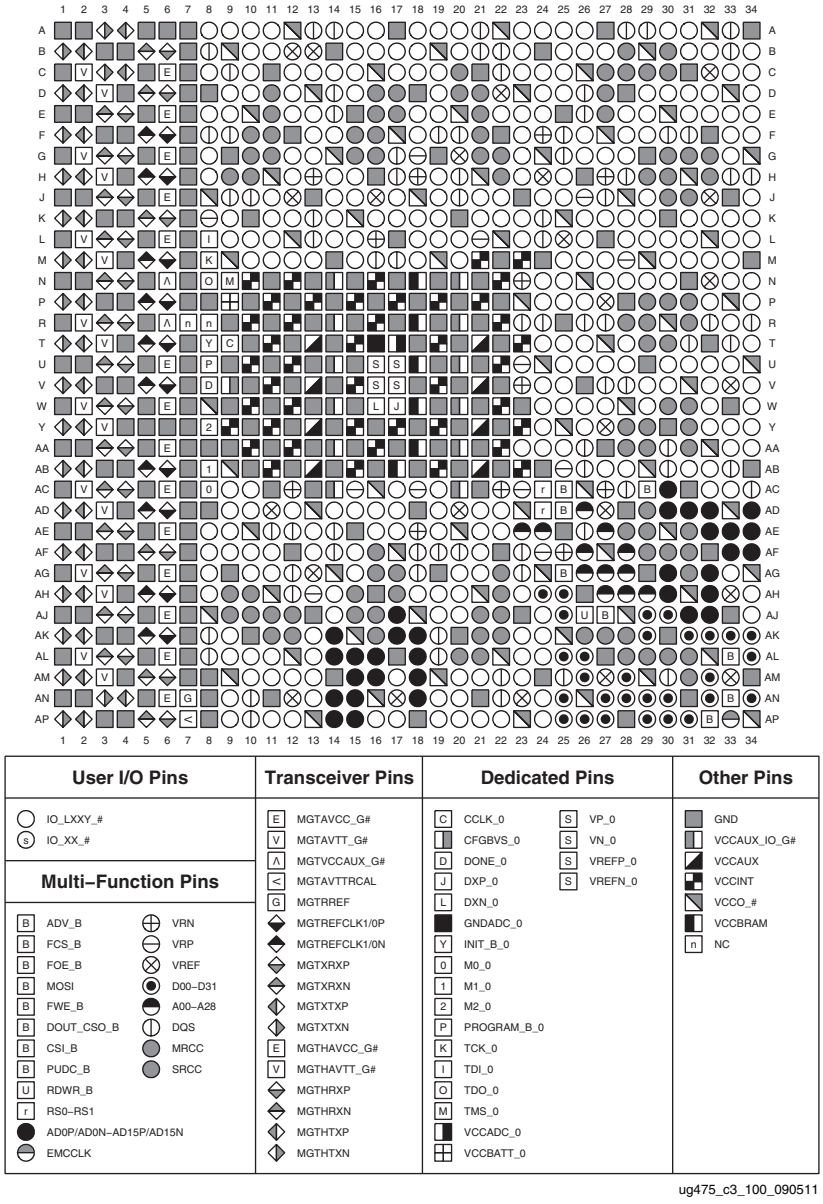


Figure 3-69: **FFG1157 Package—XC7VX485T Pinout Diagram**

www.BDTIC.com/XILINX

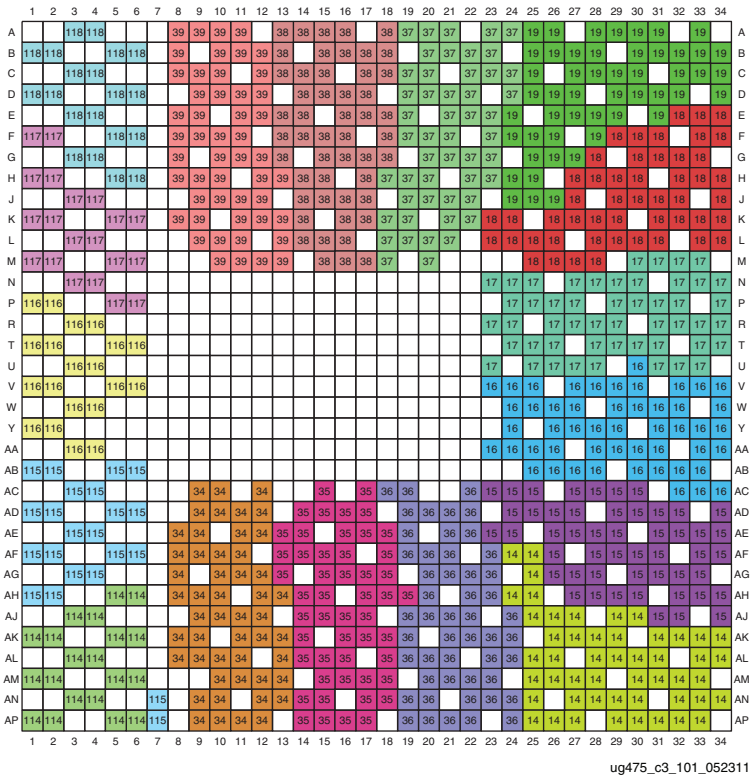


Figure 3-70: **FFG1157 Package—XC7VX485T I/O Banks**

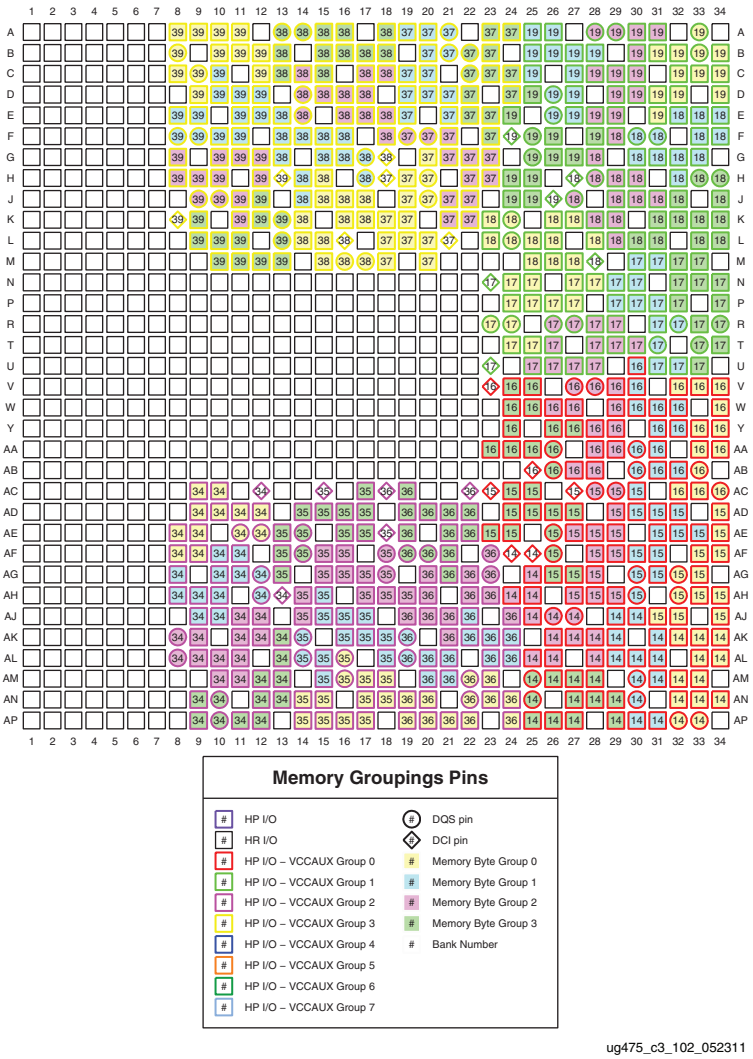


Figure 3-71: **FFG1157 Package—XC7VX485T Memory Groupings**

www.BDTIC.com/XILINX

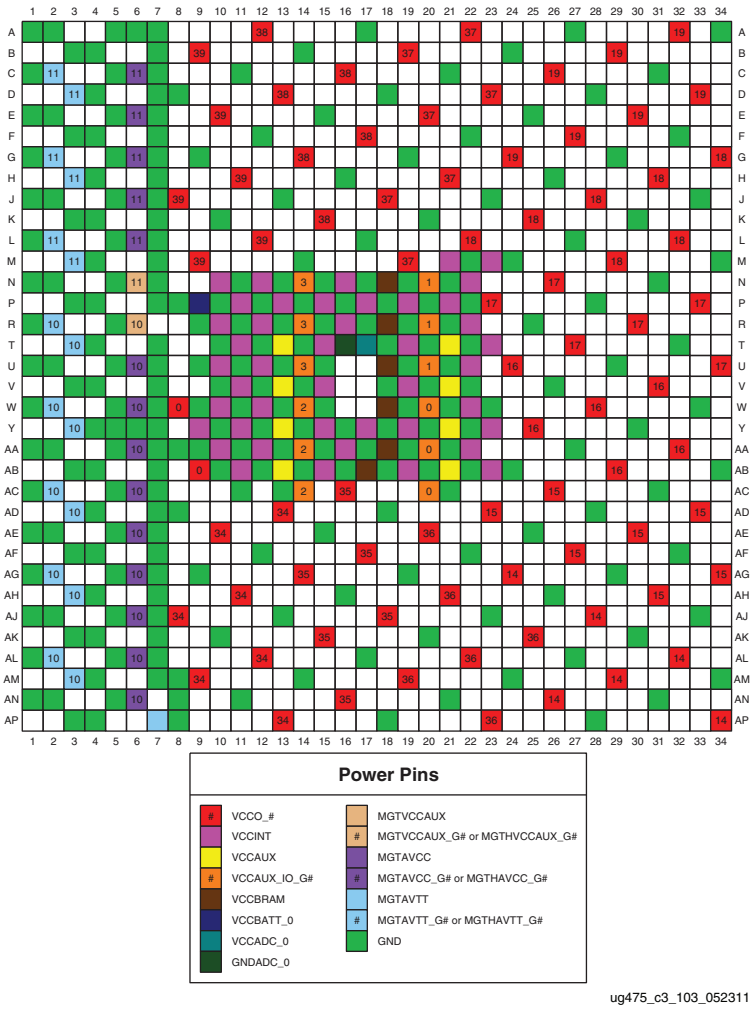
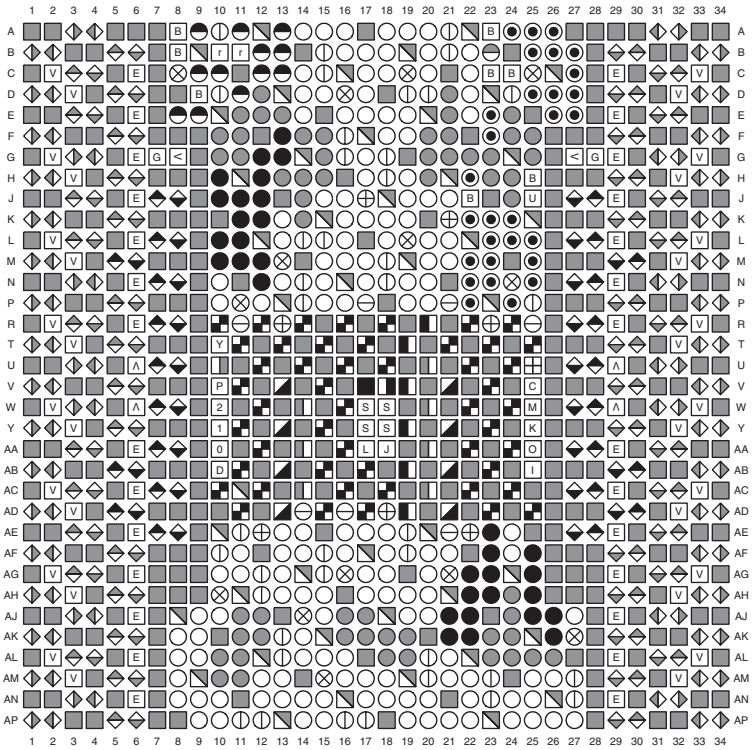


Figure 3-72: **FFG1157 Package—XC7VX485T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1158 Package—XC7VX485T



User I/O Pins	Transceiver Pins	Dedicated Pins	Other Pins
IO_LXXY_# IO_XX_#	MGTAVCC_G# MGTAVTT_G# MGTVCCAUX_G# MGTAVTTRCAL MGTRREF MGTREFCLK1/0P MGTREFCLK1/0N MGTXRXP MGTXRXN MGTXTXP MGTXTXN MGTHAVCC_G# MGTHAVTT_G# MGTHRXP MGTHRXN MGTHTXP MGTHTXN	CCLK_0 CFGBVS_0 DONE_0 DXP_0 DXN_0 GNDADC_0 INIT_B_0 M0_0 M1_0 M2_0 PROGRAM_B_0 TCK_0 TDI_0 TDO_0 TMS_0 VCCADC_0 VCCBATT_0 VP_0 VN_0 VREFP_0 VREFN_0	GND VCCAUX_IO_G# VCCAUX VCCINT VCCO_# VCCBRAM NC
Multi–Function Pins			
ADV_B FCS_B FOE_B MOSI FWE_B DOUT_CSO_B CSI_B PUDC_B RDWR_B RS0–RS1 AD0P/AD0N–AD15P/AD15N EMCCLK	VRN VRP VREF D00–D31 A00–A28 DQS MRCC SRCC		

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Figure 3-73: **FFG1158 Package—XC7VX485T Pinout Diagram**

www.BDTIC.com/XILINX

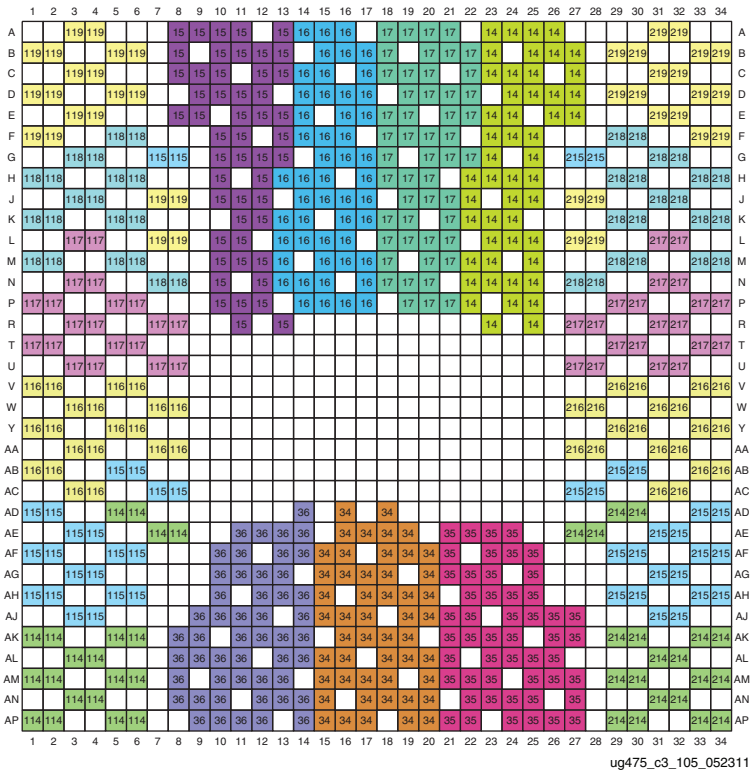

Figure 3-74: **FFG1158 Package—XC7VX485T I/O Banks**

www.BDTIC.com/XILINX

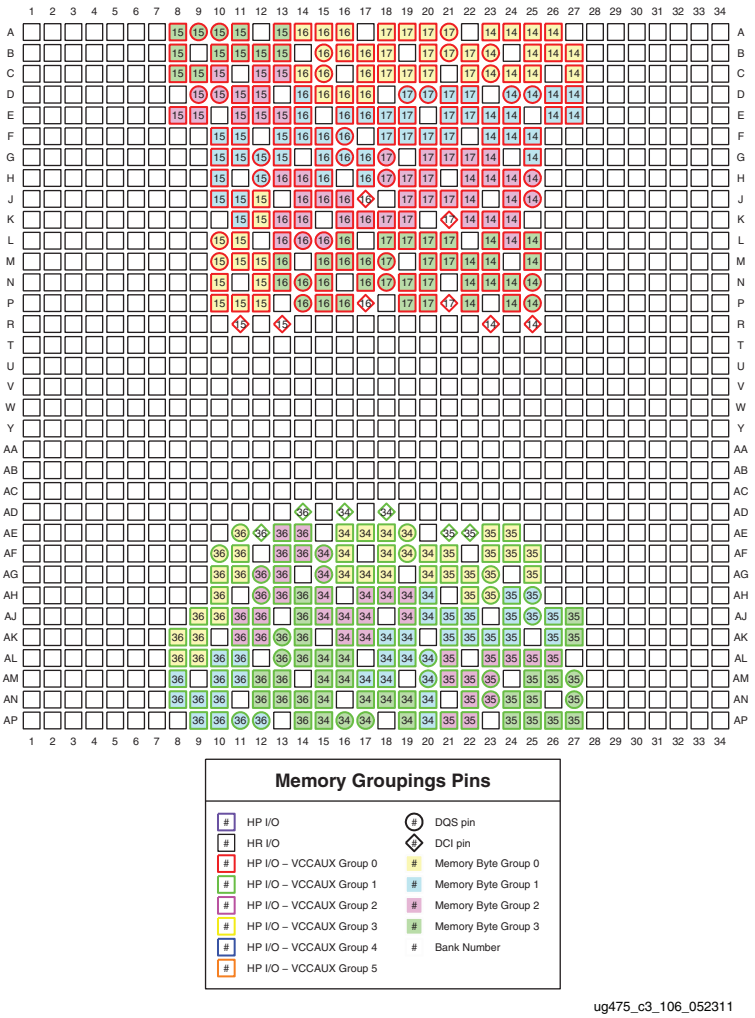

Figure 3-75: **FFG1158 Package—XC7VX485T Memory Groupings**

www.BDTIC.com/XILINX

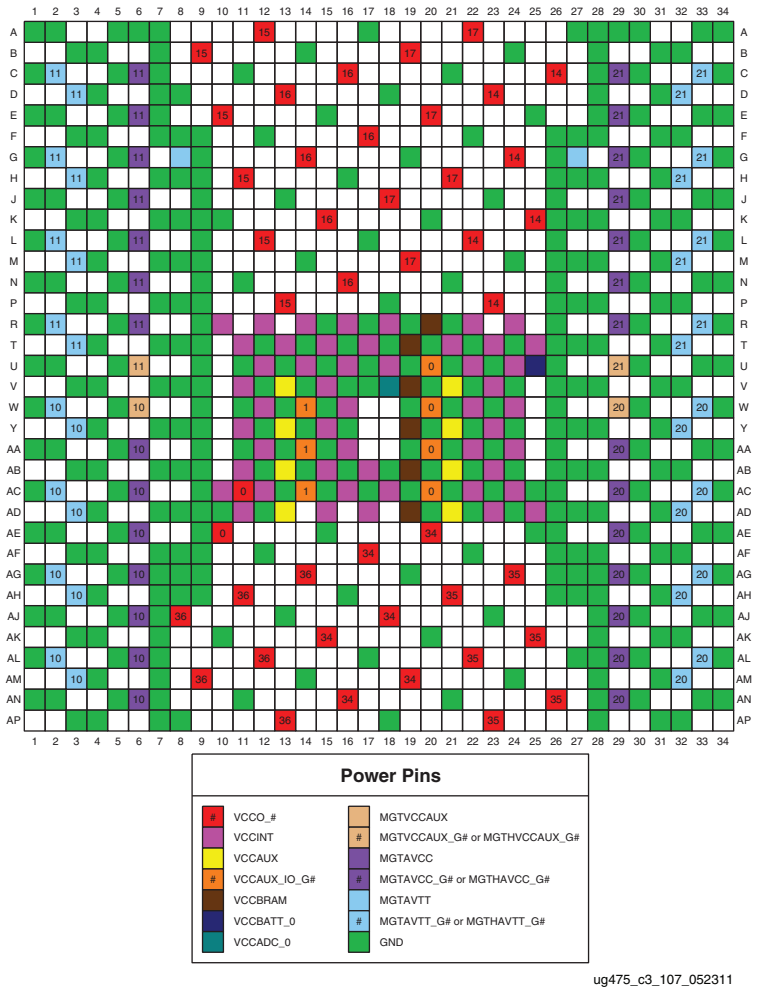

Figure 3-76: **FFG1158 Package—XC7VX485T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1761 Package—XC7VX485T

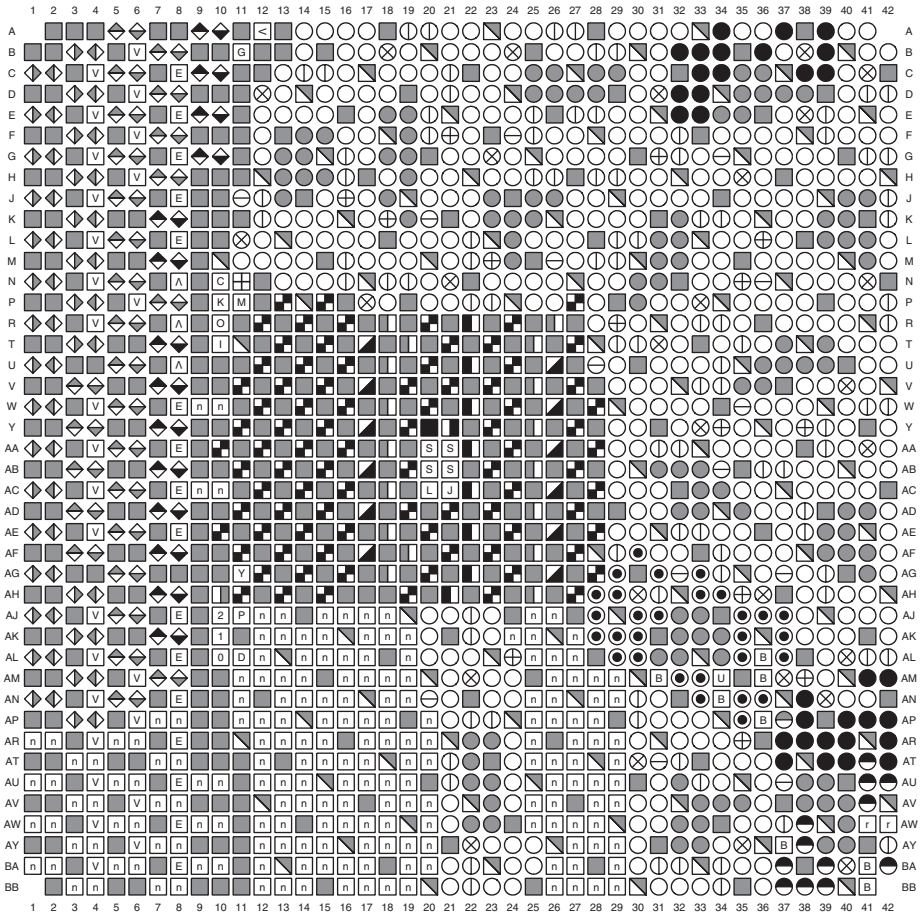

Figure 3-77: **FFG1761 Package—XC7VX485T Pinout Diagram**

www.BDTIC.com/XILINX

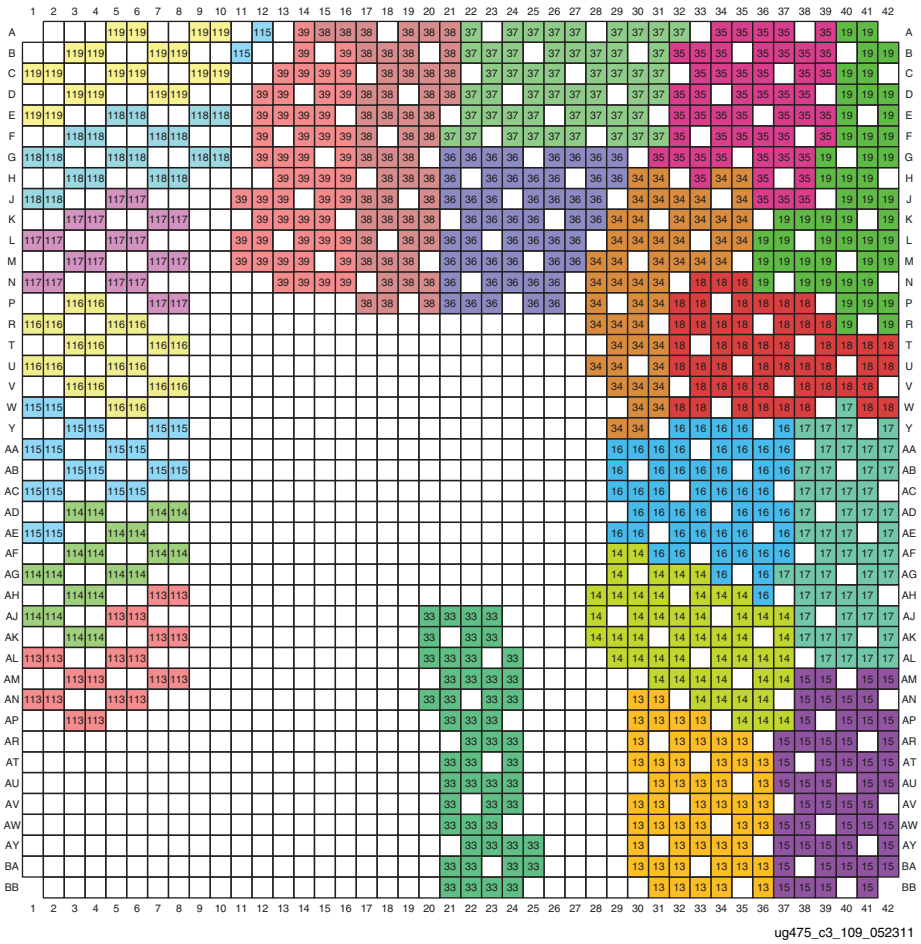

Figure 3-78: **FFG1761 Package—XC7VX485T I/O Banks**

www.BDTIC.com/XILINX

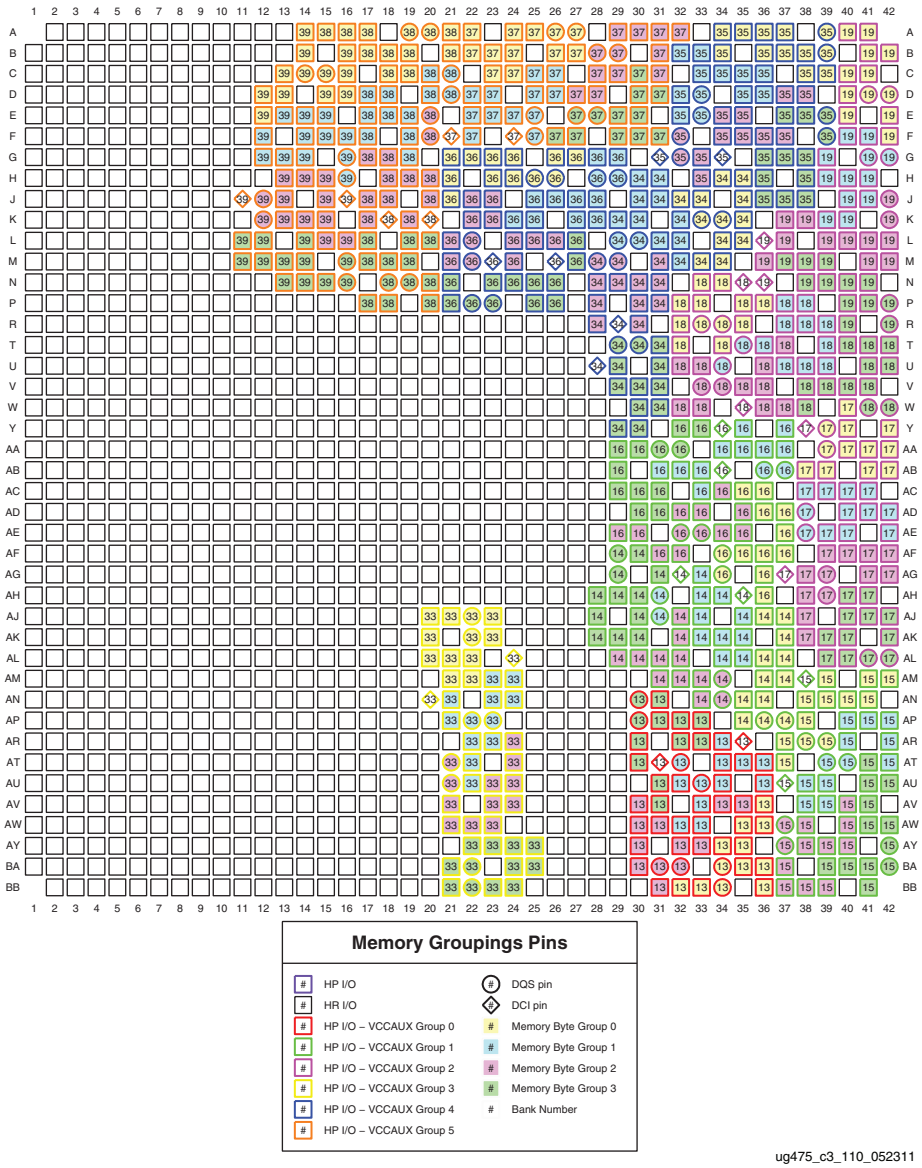

Figure 3-79: **FFG1761 Package—XC7VX485T Memory Groupings**

www.BDTIC.com/XILINX

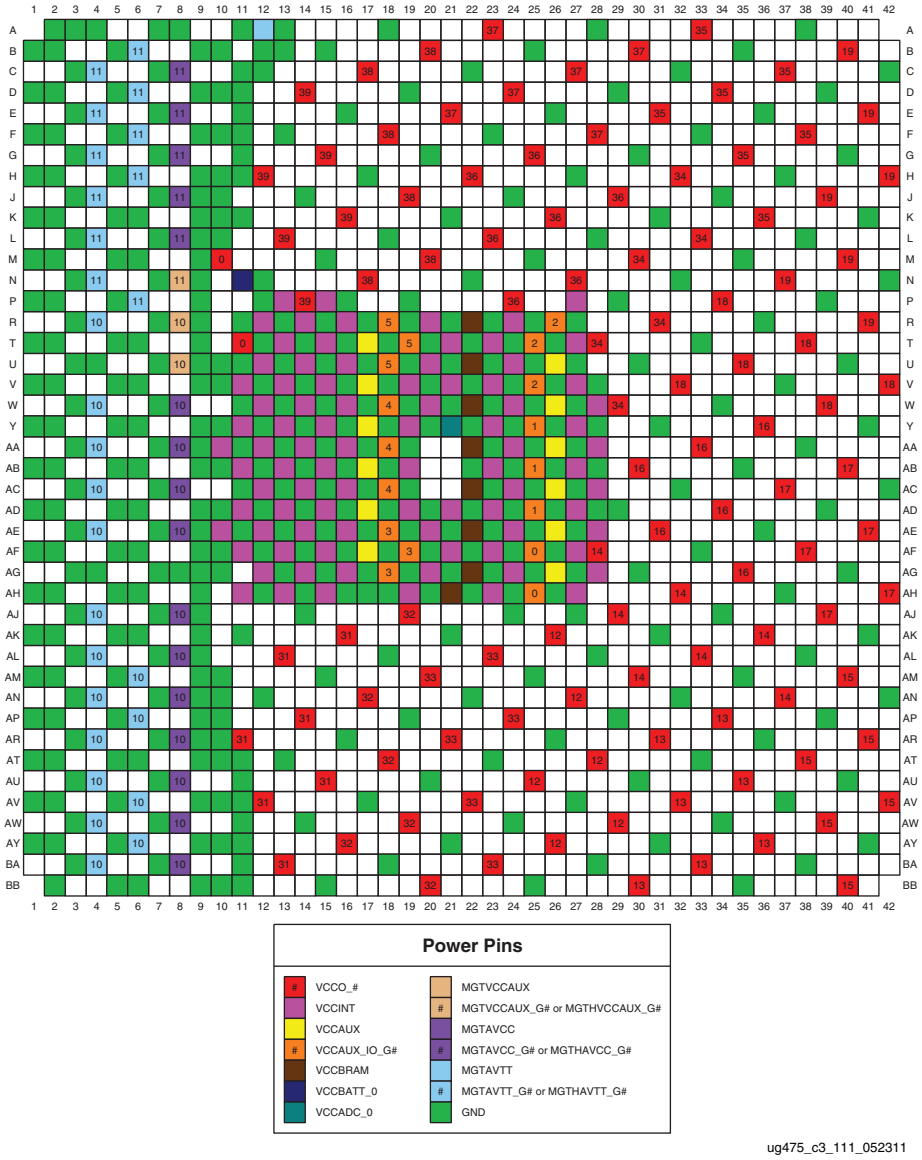

Figure 3-80: **FFG1761 Package—XC7VX485T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1927 Package—XC7VX485T

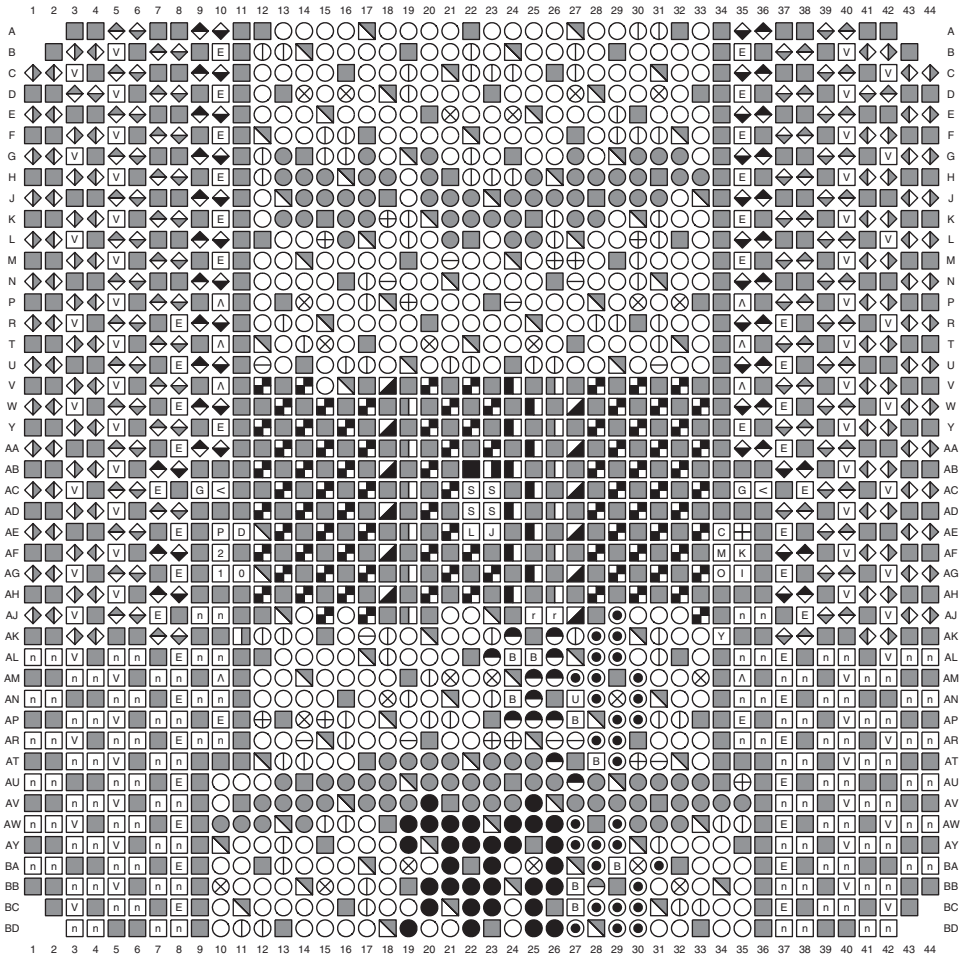

Figure 3-81: **FFG1927 Package—XC7VX485T Pinout Diagram**

www.BDTIC.com/XILINX

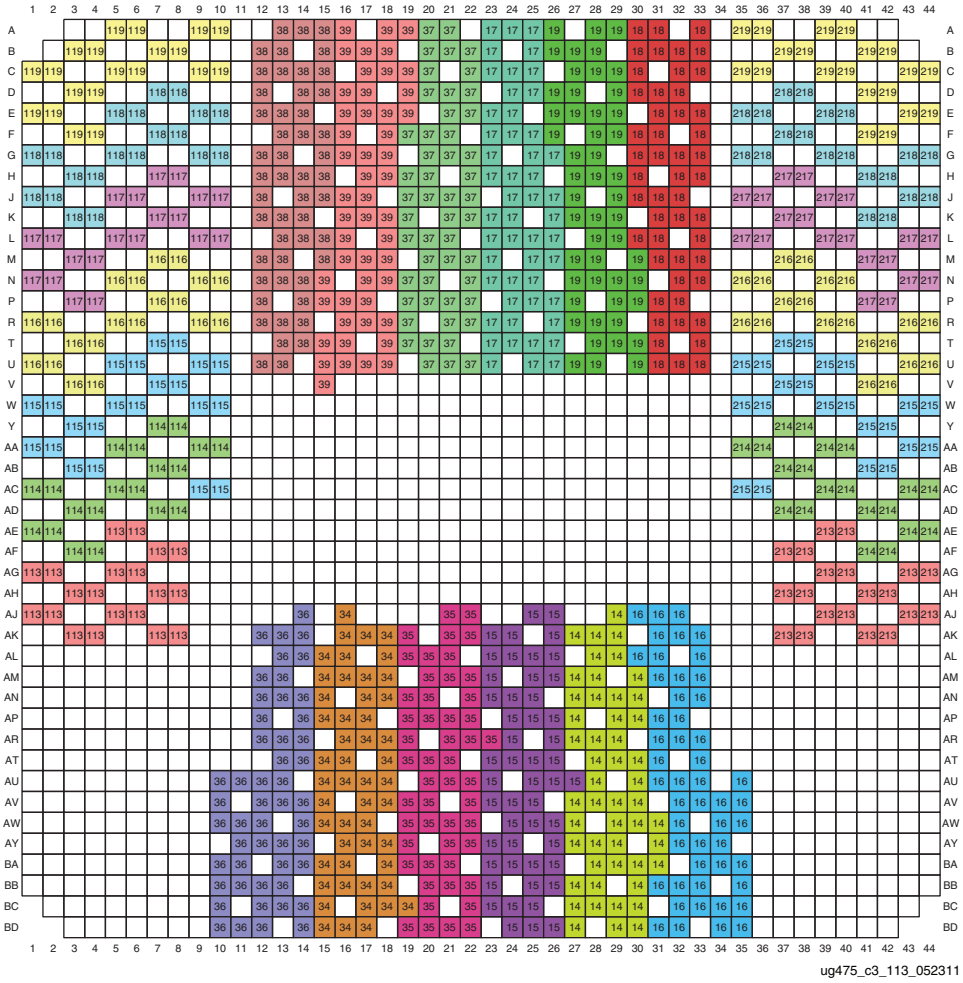

Figure 3-82: **FFG1927 Package—XC7VX485T I/O Banks**

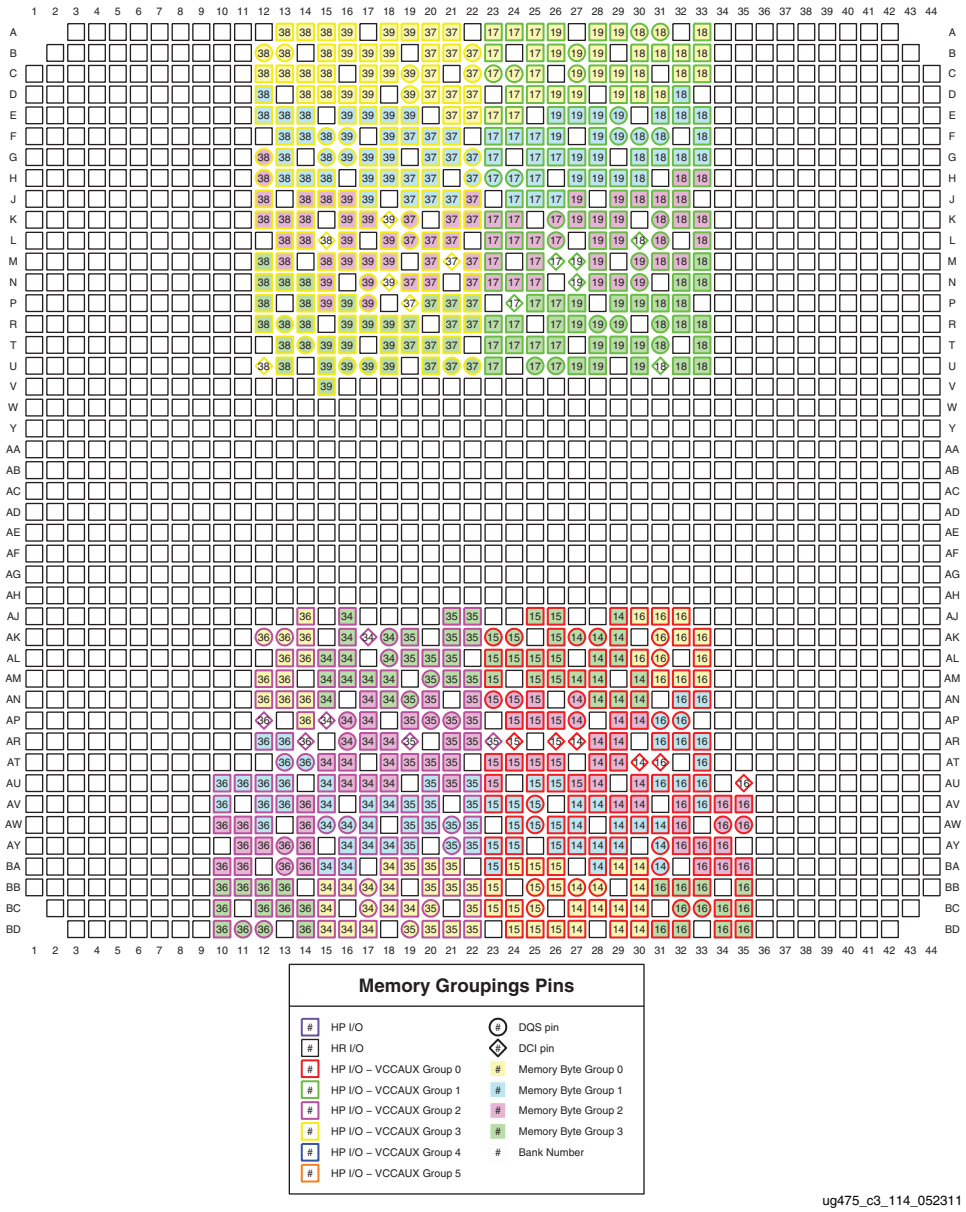

Figure 3-83: **FFG1927 Package—XC7VX485T Memory Groupings**

www.BDTIC.com/XILINX

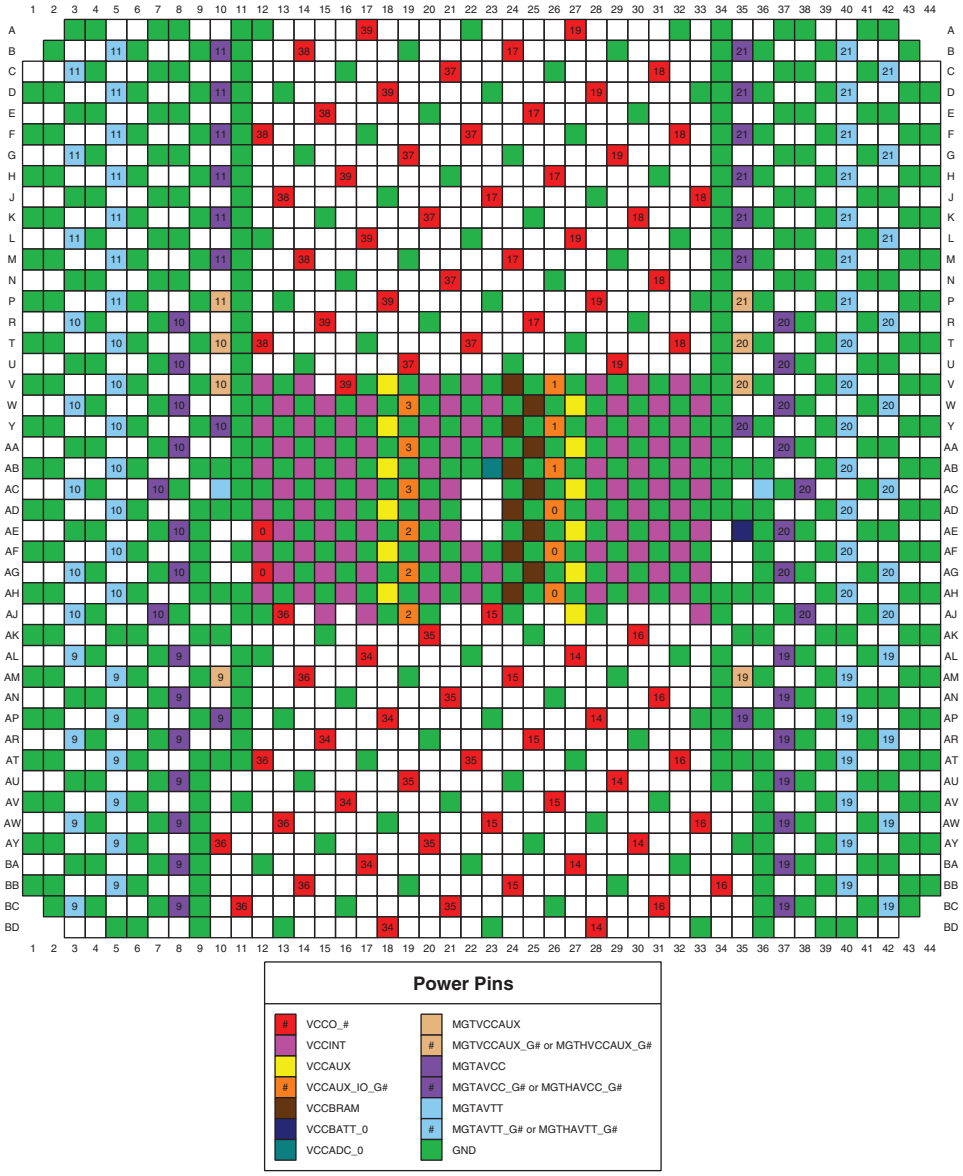

Figure 3-84: **FFG1927 Package—XC7VX485T Power and GND Placement**

www.BDTIC.com/XILINX

FFG1930 Package—XC7VX485T

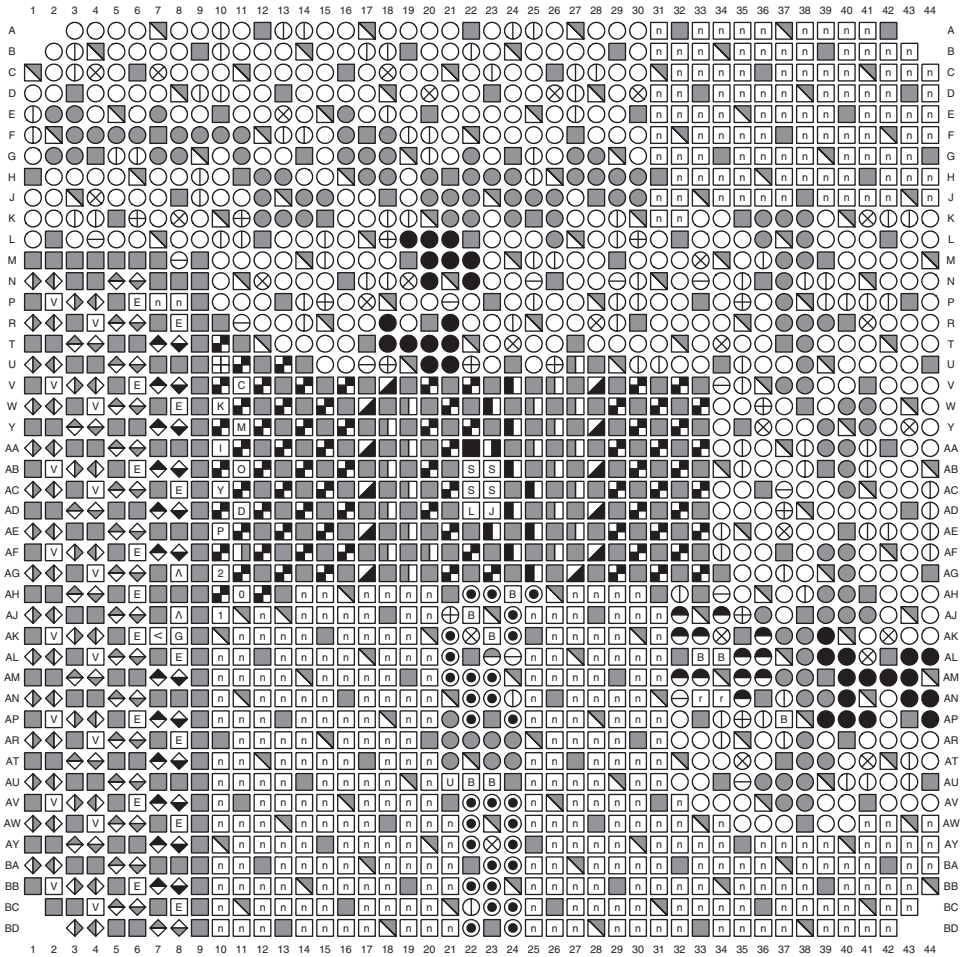

Figure 3-85: **FFG1930 Package—XC7VX485T Pinout Diagram**

www.BDTIC.com/XILINX

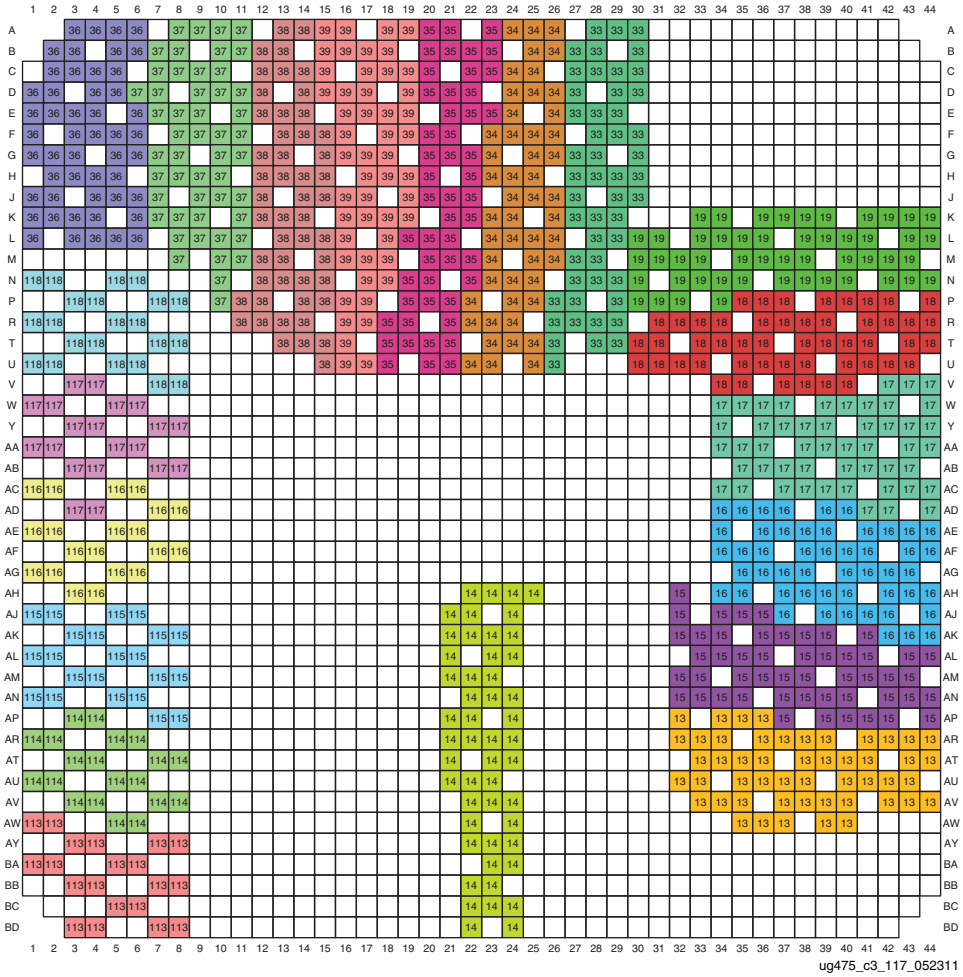

Figure 3-86: **FFG1930 Package—XC7VX485T I/O Banks**

www.BDTIC.com/XILINX

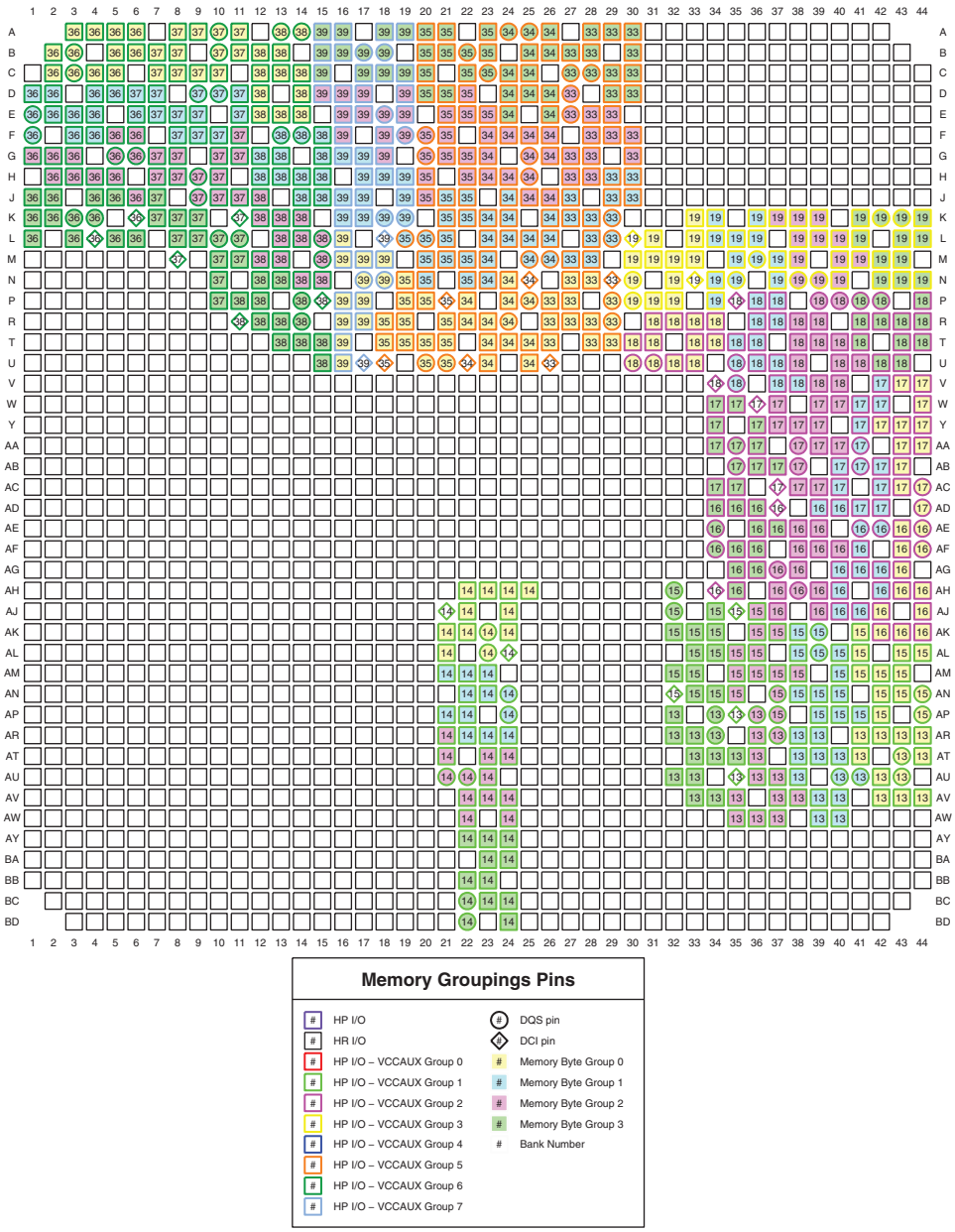

Figure 3-87: **FFG1930 Package—XC7VX485T Memory Groupings**

www.BDTIC.com/XILINX

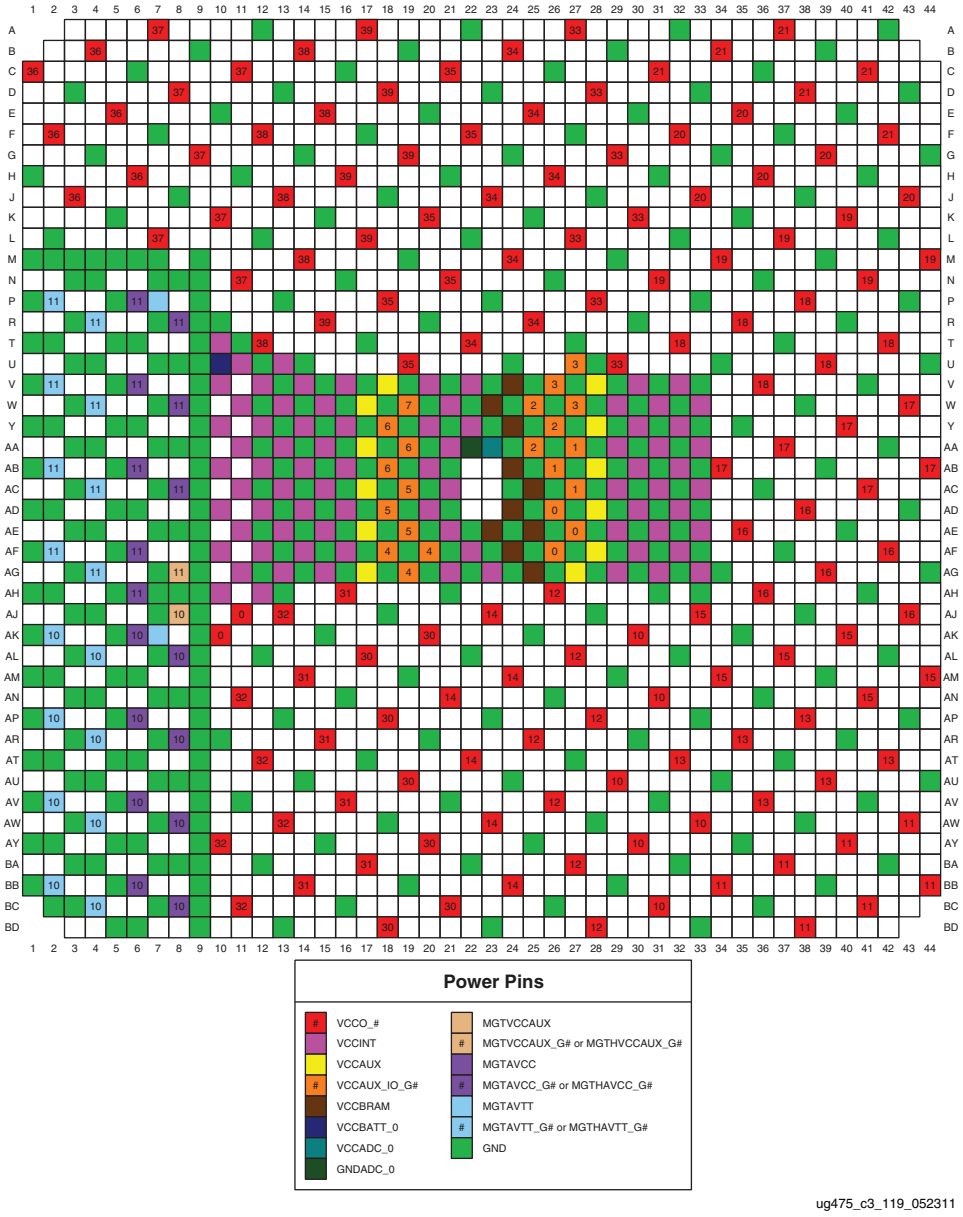

Figure 3-88: **FFG1930 Package—XC7VX485T Power and GND Placement**

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Chapter 4

Mechanical Drawings

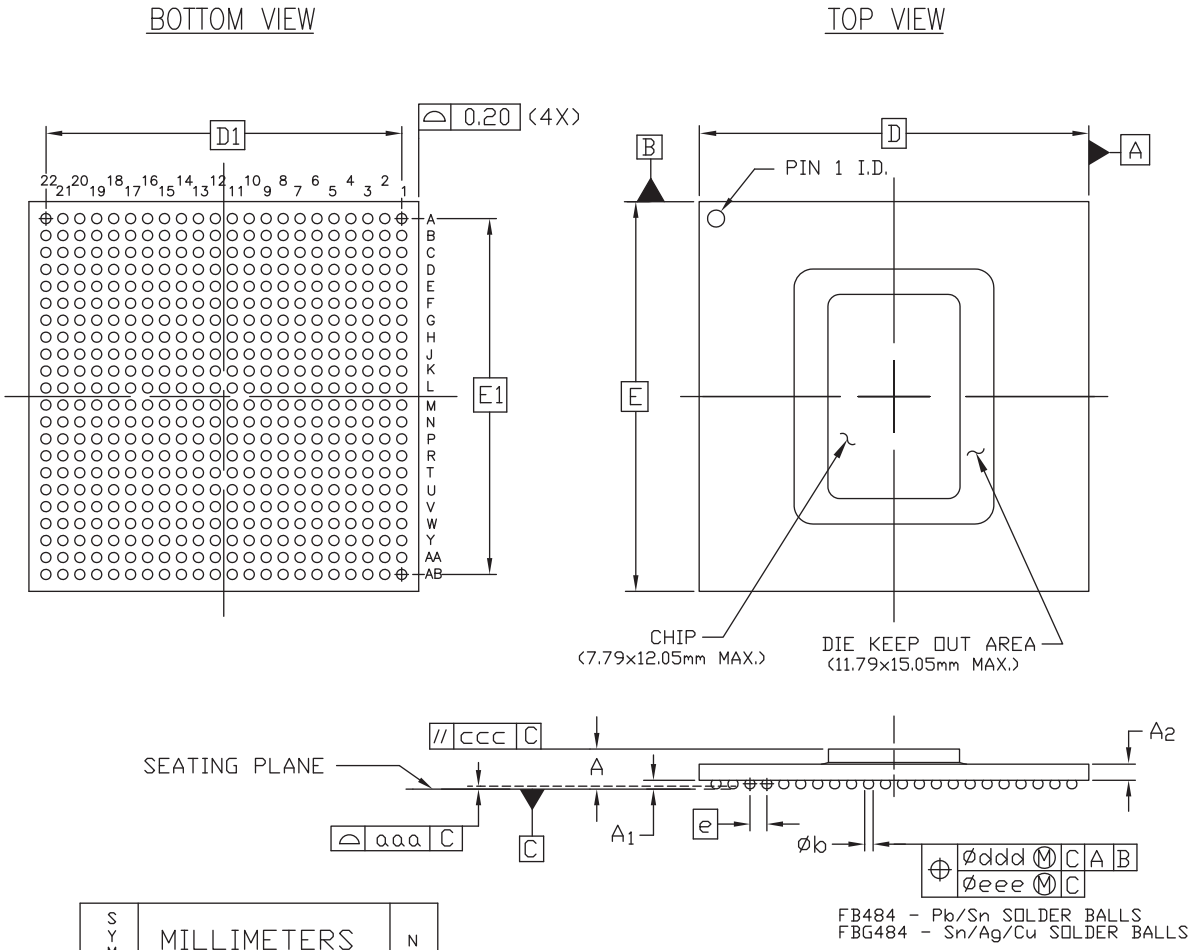
Summary

This chapter provides mechanical drawings (package specifications) of the following 7 series FPGA packages:

Note: This chapter is intentionally missing drawings.

www.BDTIC.com/XILINX

FB(G)484 Flip-Chip Bare-Die BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.07	2.37	2.67	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	23.00 BASIC			
D_1/E_1	21.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.25	
ddd			0.25	
eee			0.10	
M	26			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034

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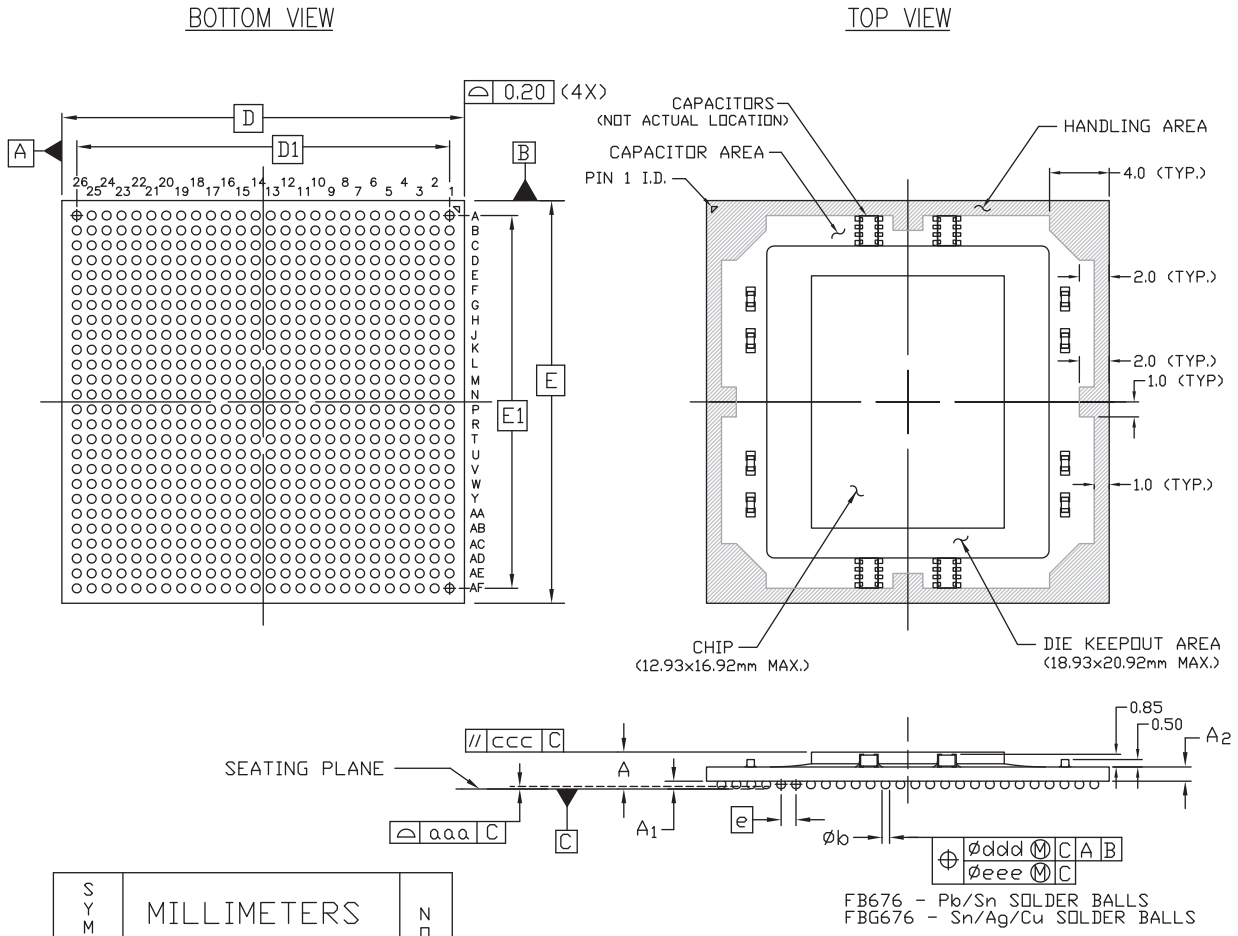
Figure 4-1: **FB(G)484 Flip-Chip Bare-Die BGA Package Specifications for Kintex-7 FPGAs**

www.BDTIC.com/XILINX

FB(G)676 Flip-Chip Bare-Die BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.07	2.37	2.67	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

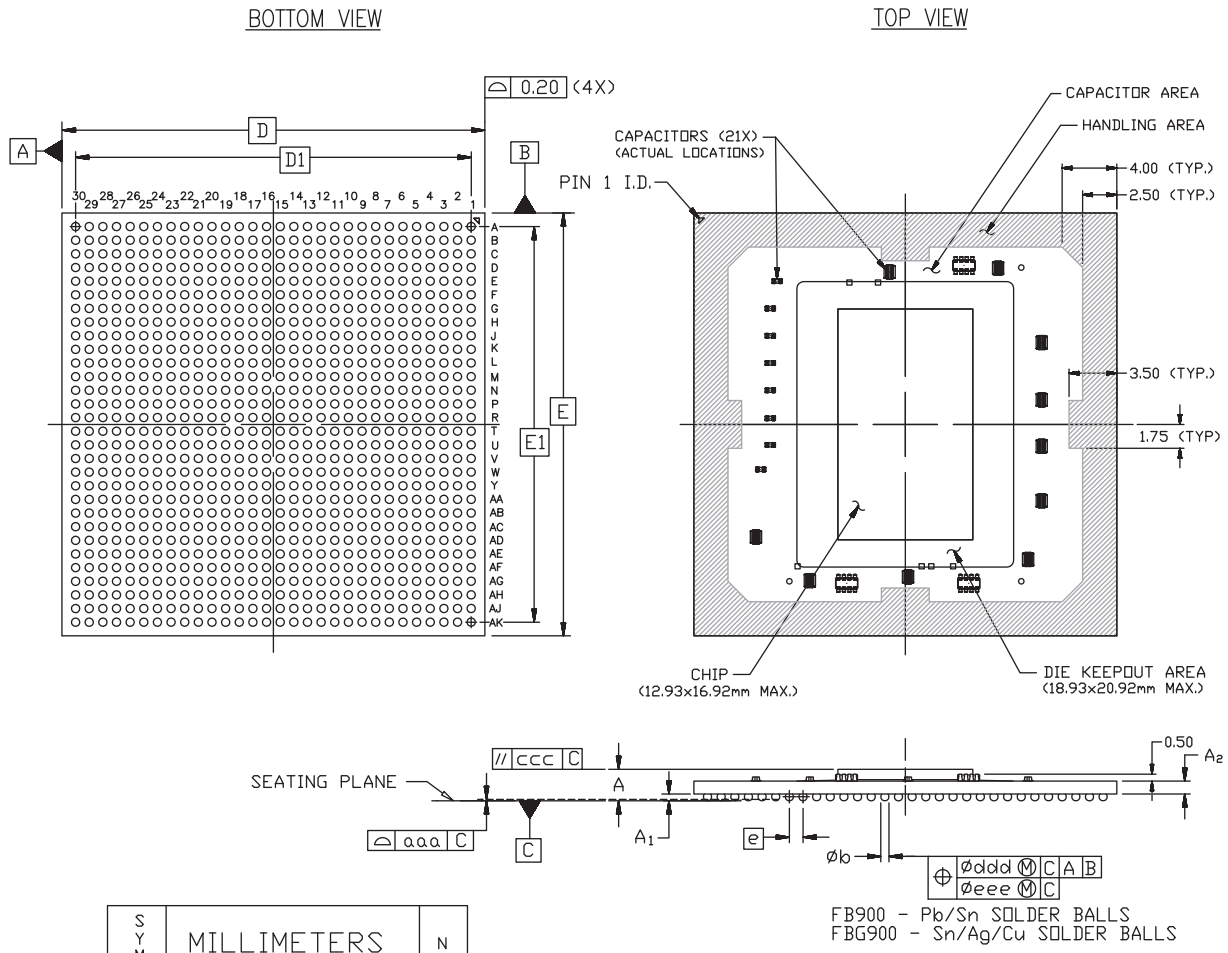
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CAPACITORS SHOWN ARE FOR ILLUSTRATION ONLY
4. CONFORMS TO JEDEC MS–034

ug475_c4_02_031511

Figure 4-2: **FB(G)676 Flip-Chip Bare-Die BGA Package Specifications for Kintex-7 FPGAs**

www.BDTIC.com/XILINX

FB(G)900 Flip-Chip Bare-Die BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.04	2.34	2.64	
A_1	0.40	0.50	0.60	
A_2	0.88	0.98	1.08	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
ccc			0.35	
ddd			0.30	
eee			0.10	
M	30			2

NOTES:

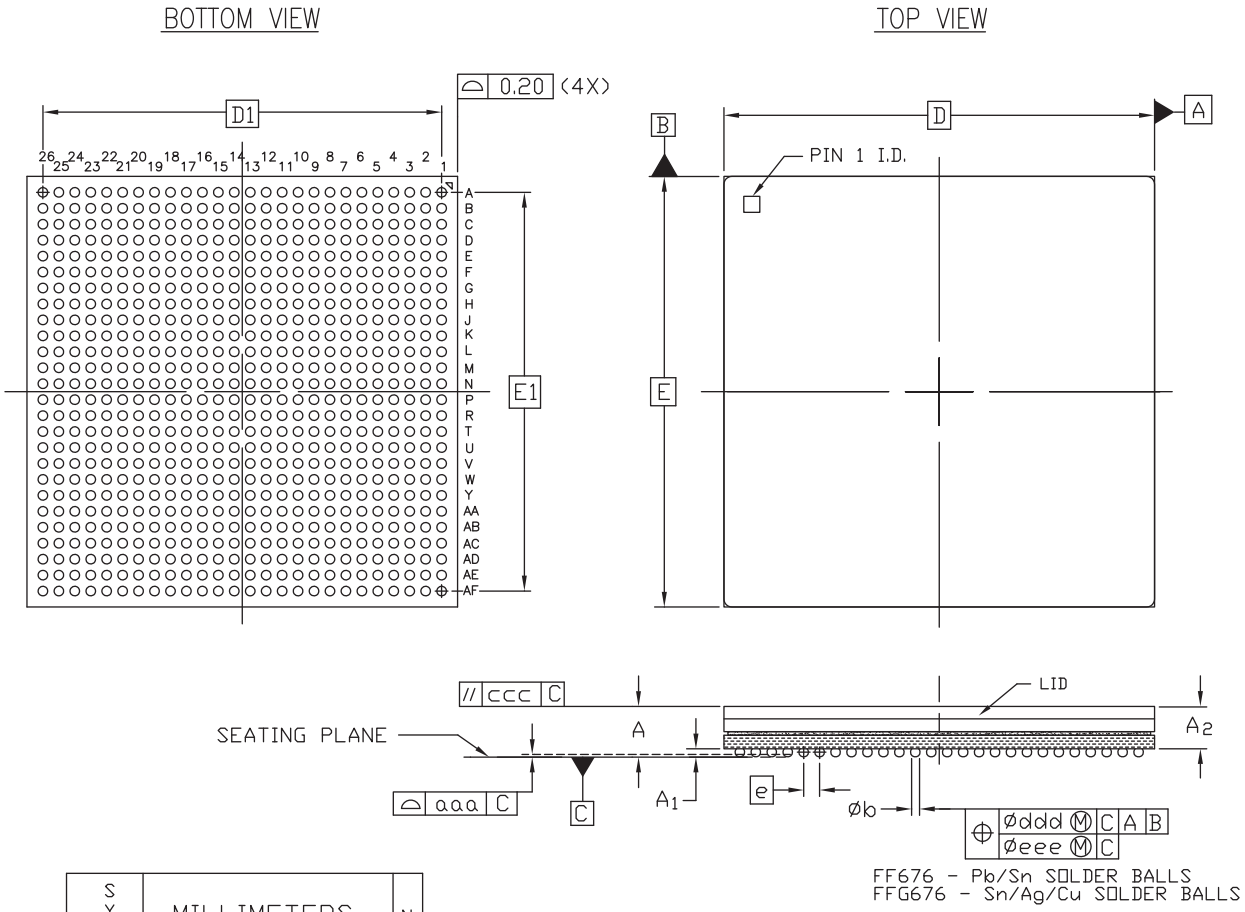
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CAPACITORS SHOWN ARE ACTUAL LOCATION
4. CONFORMS TO JEDEC MS-034 (DEPOPULATED)

ug475_c4_03_031511

Figure 4-3: **FB(G)900 Flip-Chip Bare-Die BGA Package Specifications for Kintex-7 FPGAs**

www.BDTIC.com/XILINX

FF(G)676 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.85	3.15	3.45	
A_1	0.40	0.50	0.60	
A_2	2.45	~	2.85	
D/E	27.00 BASIC			
D_1/E_1	25.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.25	
ddd	~	~	0.25	
eee	~	~	0.10	
M	26			2

NOTES:

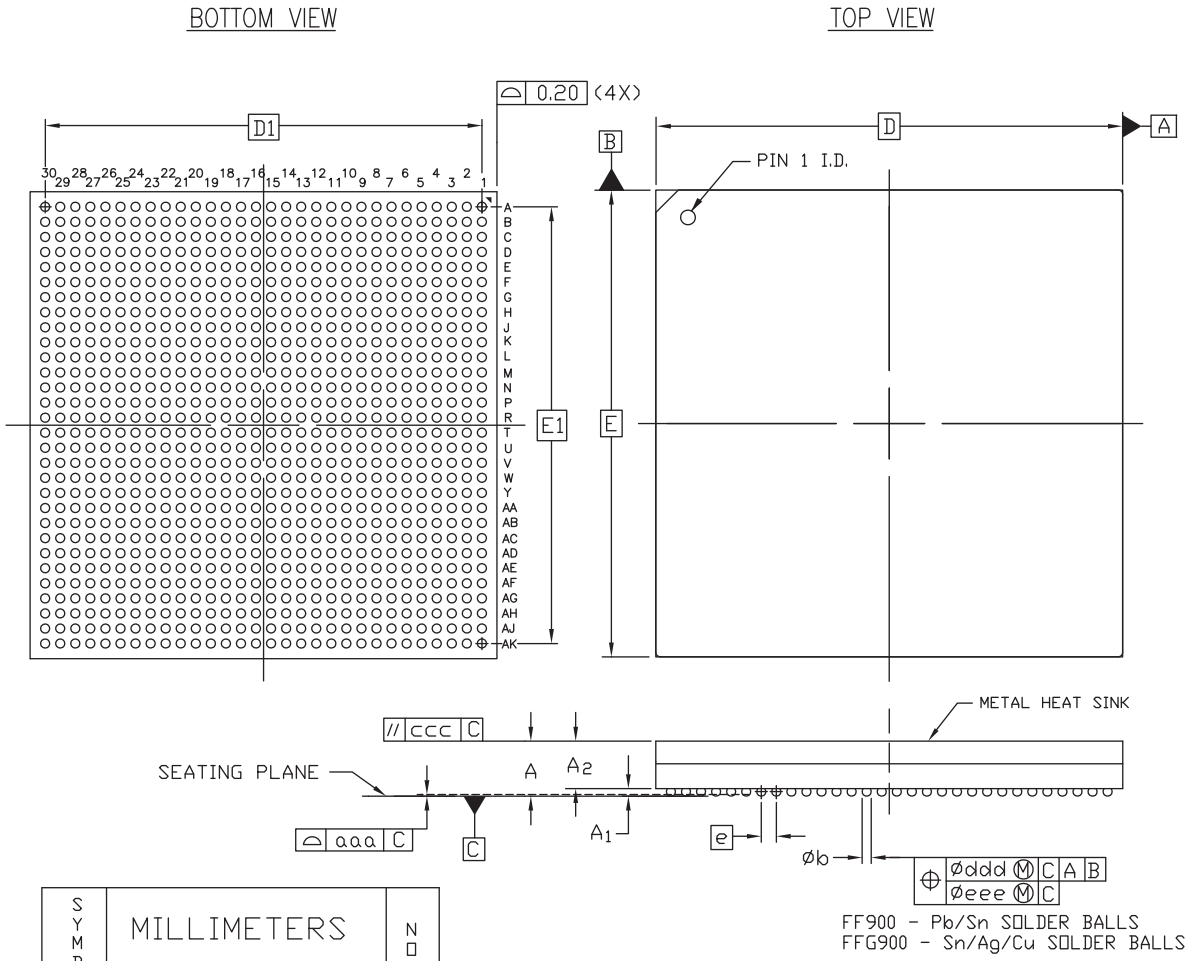
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAL-1

ug475_c4_04_031511

Figure 4-4: **FF(G)676 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

www.BDTIC.com/XILINX

FF(G)900 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.85	3.15	3.45	
A_1	0.40	0.50	0.60	
A_2	2.45	~	2.85	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAN–1

ug475_c4_05_031511

Figure 4-5: **FF(G)900 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

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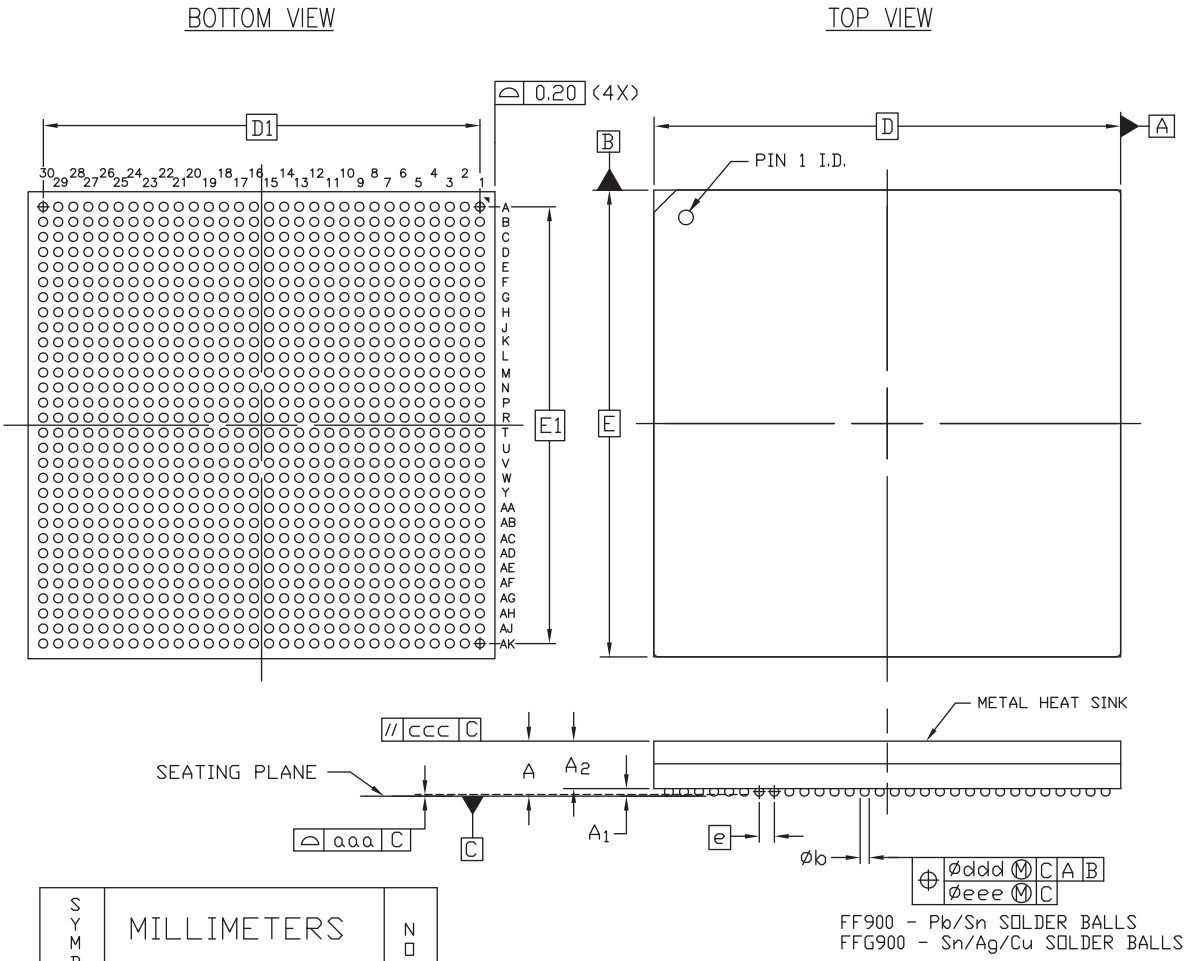
FF(G)901 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.85	3.15	3.45	
A_1	0.40	0.50	0.60	
A_2	2.45	~	2.85	
D/E	31.00 BASIC			
D_1/E_1	29.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~	~	0.20	
ccc	~	~	0.35	
ddd	~	~	0.30	
eee	~	~	0.10	
M	30			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS-034-AAN-1

ug475_c4_06_031511

Figure 4-6: **FF(G)901 Flip-Chip BGA Package Specifications for Kintex-7 FPGAs**

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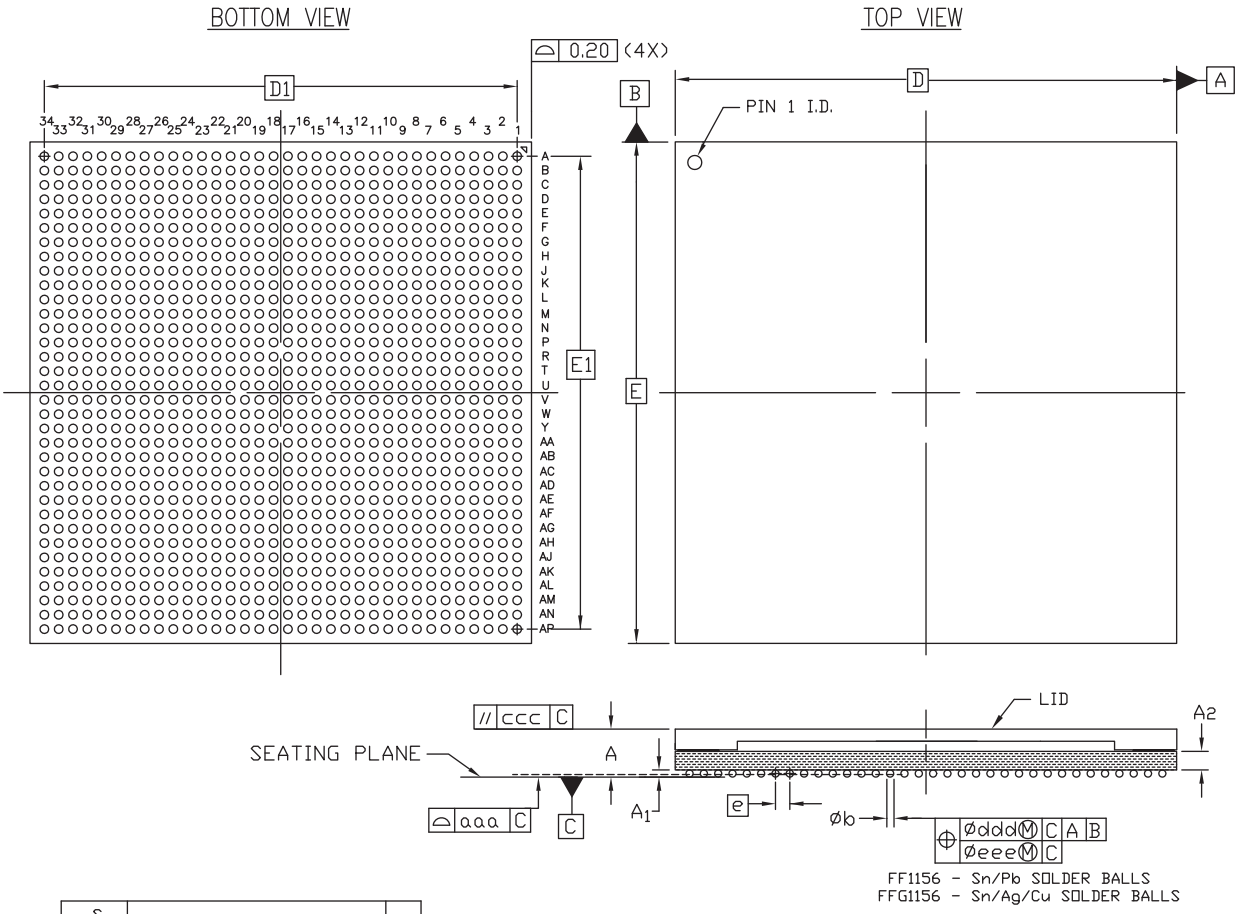
FF(G)1156 Flip-Chip BGA (Kintex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	2.70	~~	3.50	
A_1	0.40	0.50	0.60	
A_2	0.90	~~	1.50	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	4
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M–1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE
3. CONFORMS TO JEDEC MS–034–AAR–1
4. ACTUAL SOLDER BALL COUNT = 1156
5. THIS PACKAGE IS USED FOR KINTEX®–7 FPGAS REFER TO PK384 FOR THE MECHANICAL DRAWING OF THE FF1156 PACKAGE USED FOR VIRTEX®5 FPGAS AND PK401 FOR VIRTEX®–6 FPGAS

ug475_c4_07_052311

Figure 4-7: **FF(G)1156 Flip-Chip BGA Package Specification for Kintex-7 FPGAs**

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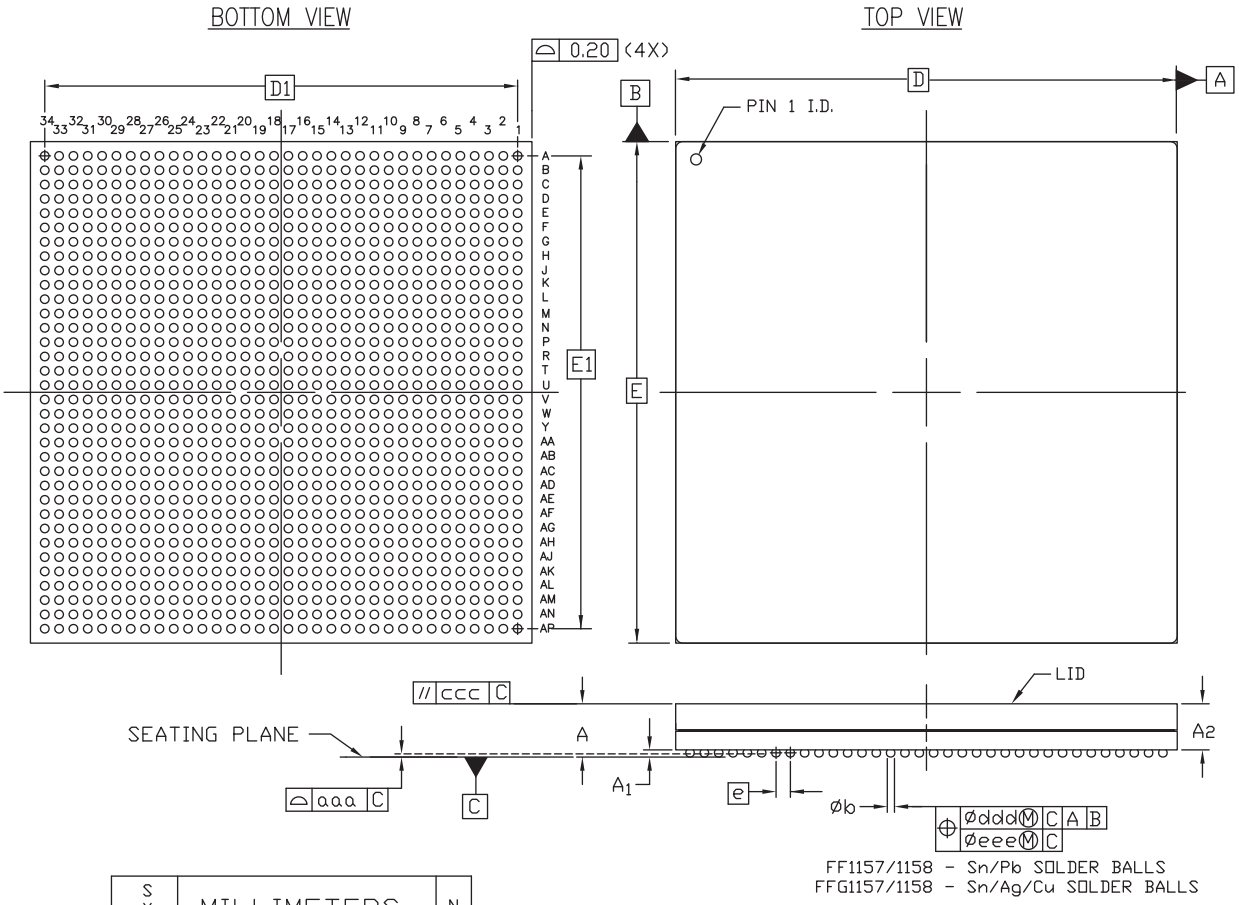
FF(G)1157 and FF(G)1158 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.00	~~	3.60	
A_1	0.40	0.50	0.60	
A_2	2.60	~~	3.00	
D/E	35.00 BASIC			
D_1/E_1	33.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa	~~	~~	0.20	
ccc	~~	~~	0.35	
ddd	~~	~~	0.30	
eee	~~	~~	0.10	
M	34			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1994
2. SYMBOL 'M' IS THE BALL MATRIX SIZE.
3. CONFORMS TO JEDEC MS-034-AAR-1
4. ACTUAL SOLDER BALL COUNT = 1156

ug475_c4_08_052311

Figure 4-8: **FF(G)1157 and FF(G)1158 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

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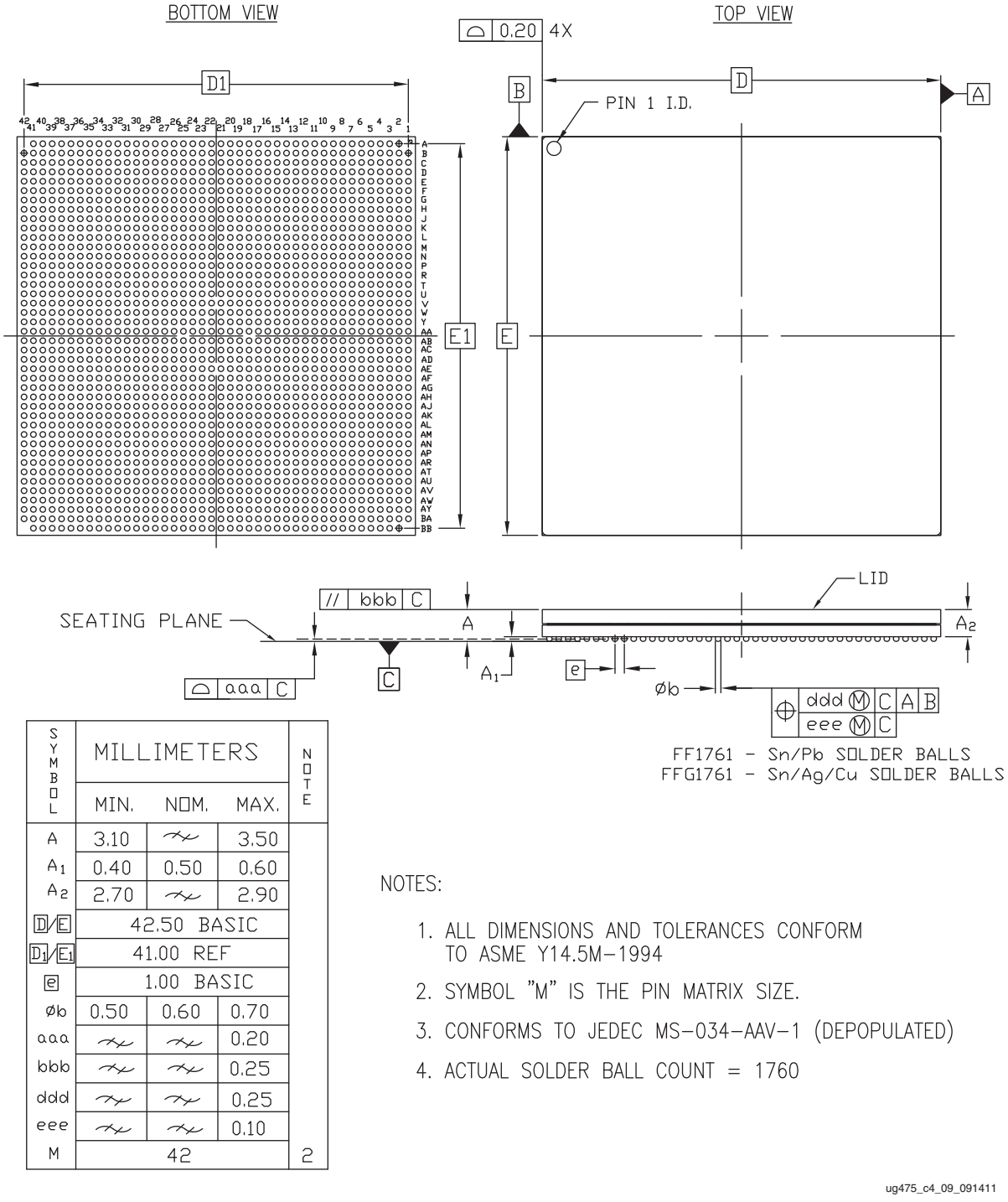
FF(G)1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.10		3.50	
A_1	0.40	0.50	0.60	
A_2	2.70		2.90	
D/E	42.50 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_09_091411

Figure 4-9: **FF(G)1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

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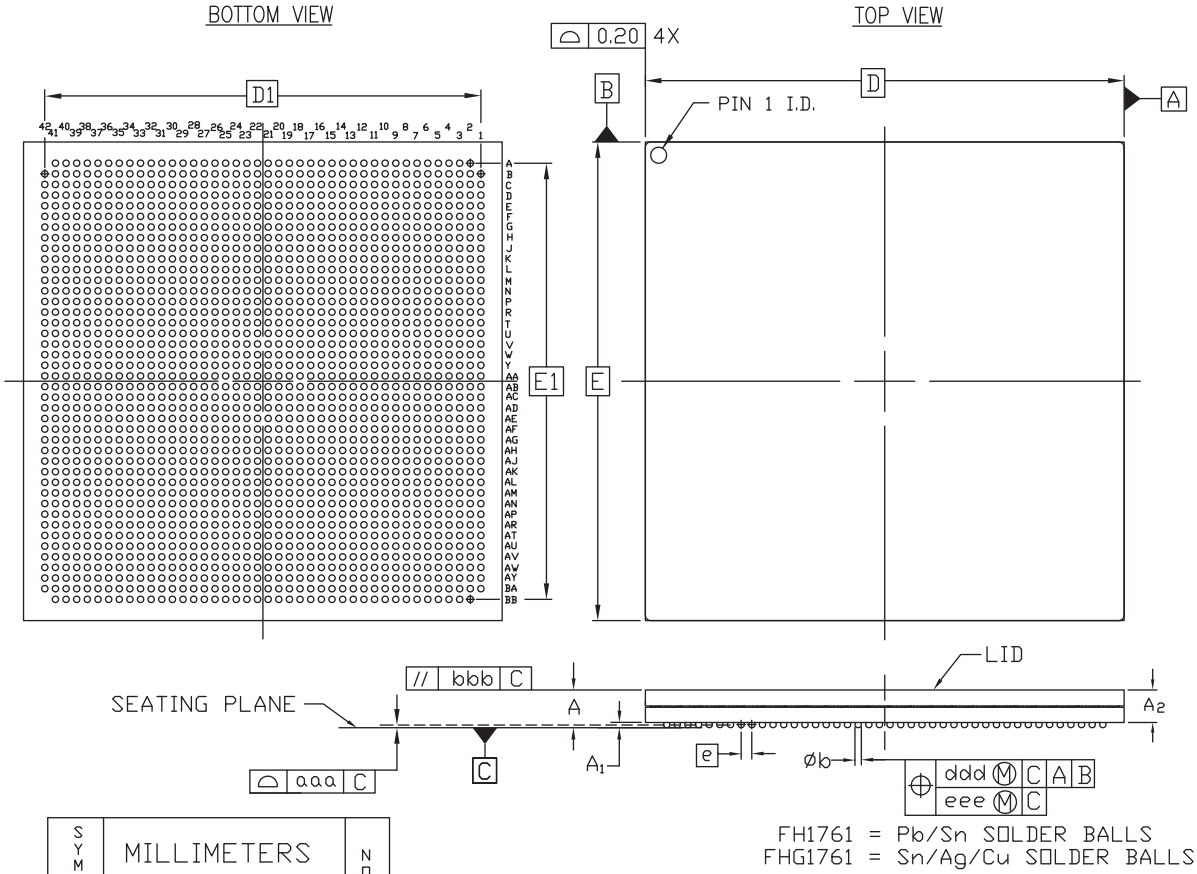
FH(G)1761 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	41.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	42			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. CONFORMS TO JEDEC MS–034–AAV–1 (DEPOPULATED)
4. ACTUAL SOLDER BALL COUNT = 1760

ug475_c4_10_100311

Figure 4-10: **FF(G)1761 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

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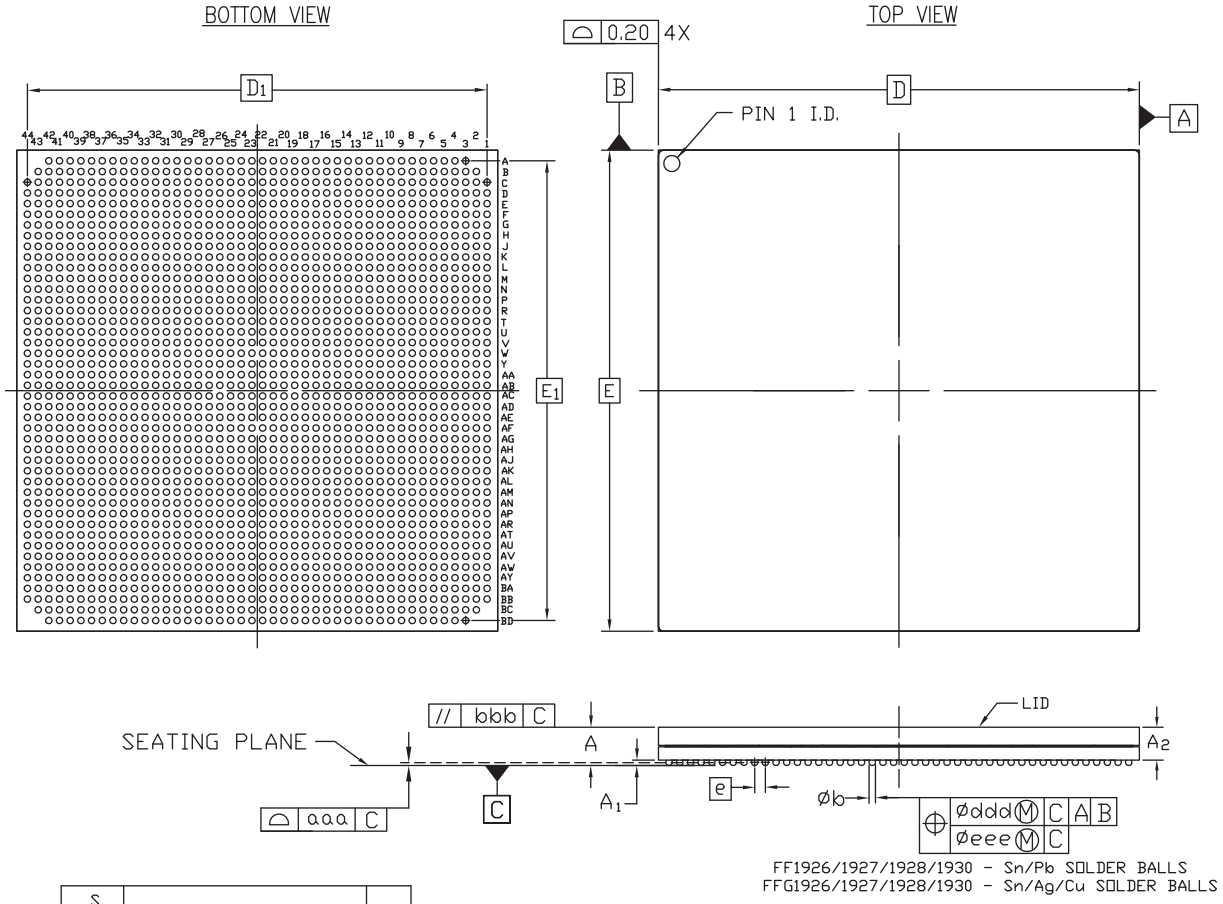
FF(G)1926, FF(G)1927, FF(G)1928, and FF(G)1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS			NOTE
	MIN.	NOM.	MAX.	
A	3.25		3.65	
A_1	0.40	0.50	0.60	
A_2	2.90		3.20	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924
4. CONFORMS TO JEDEC MS–034–AAW–1 (DEPOPULATED)

ug475_c4_11_100311

Figure 4-11: **FF(G)1926, FF(G)1927, FF(G)1928, and FF(G)1930 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

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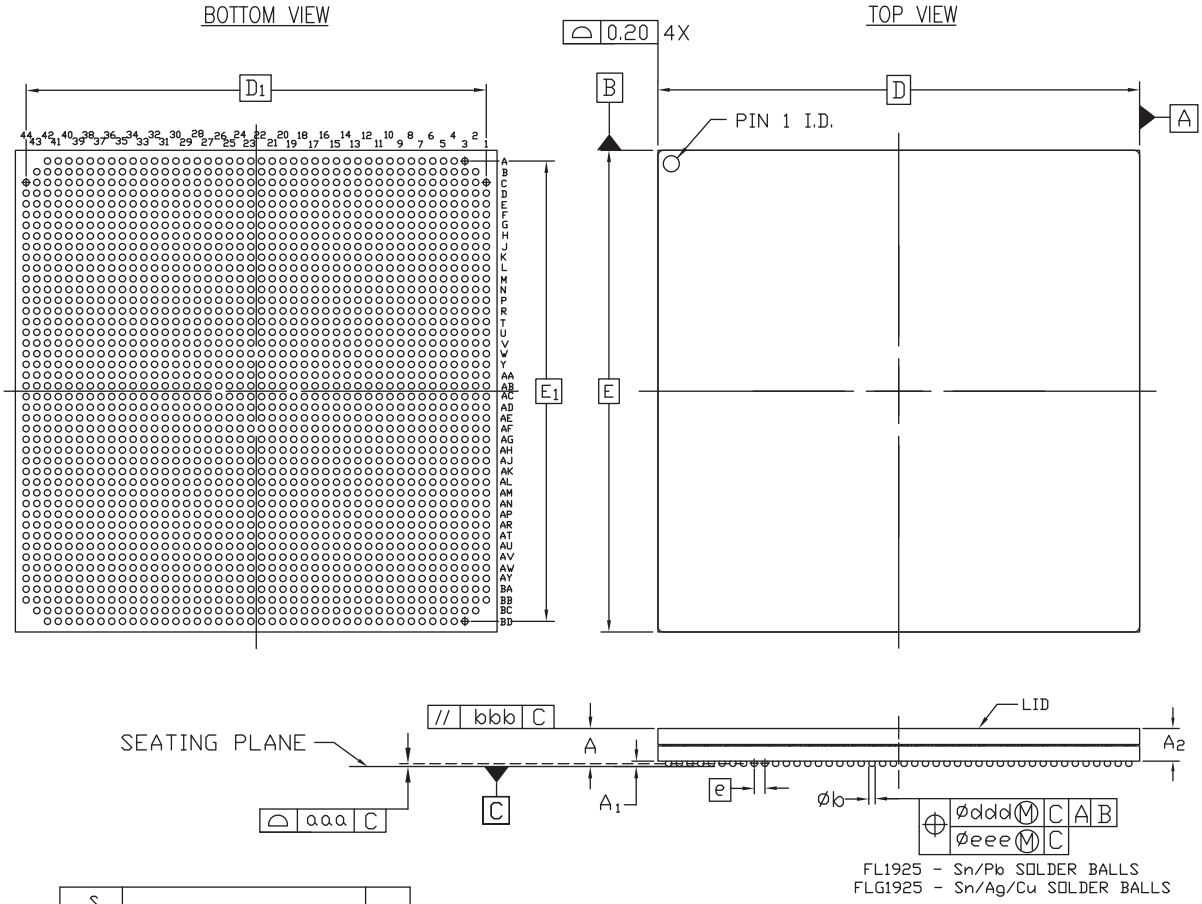
FL(G)1925, FL(G)1928, and FL(G)1930 Flip-Chip BGA (Virtex-7 FPGAs) (1.0 mm Pitch)



SYMBOL	MILLIMETERS MIN.	NOM.	MAX.	NOTE
A	3.25		3.75	
A_1	0.40	0.50	0.60	
A_2	2.85		3.15	
D/E	45.00 BASIC			
D_1/E_1	43.00 REF			
e	1.00 BASIC			
øb	0.50	0.60	0.70	3
aaa			0.20	
bbb			0.25	
ddd			0.25	
eee			0.10	
M	44			2

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994
2. SYMBOL "M" IS THE PIN MATRIX SIZE.
3. ACTUAL SOLDER BALL COUNT = 1924

ug475_c4_12_100311

Figure 4-12: **FL(G)1925, FL(G)1928, and FL(G)1930 Flip-Chip BGA Package Specification for Virtex-7 FPGAs**

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Chapter 5

Thermal Specifications

Summary

This chapter provides thermal data associated with 7 series FPGAs packages. The following topics are discussed:

- Introduction
- Power Management Strategy
- Some Thermal Management Options
- Support for Compact Thermal Models (CTM)
- References

Introduction

7 series FPGAs are offered exclusively in thermally efficient flip-chip BGA packages. These 0.5 mm, 0.8 mm, and 1.0 mm flip-chip packages range in pin-count from the smaller 10 x 10 mm CPG236 to the 45 x 45 mm FFG1930. The suite of packages is used to address the various power requirements of the 7 series devices. All 7 series devices are implemented in the 28 nm process technology.

Similar to Virtex®-6 FPGAs, all 7 series devices feature the versatile SelectIO™ resources that support a variety of I/O standards. They also include analog-to-digital converters (XADC), DSPs, and other traditional features and blocks (such as block RAM) contained in earlier Virtex products.

In line with Moore's law, the transistor count in this family of devices has been increased substantially. Though several innovative features at the silicon level have been deployed to minimize power dissipation, including leakage at the 28 nm node, these products have more densely packed transistors and embedded blocks with the capability to run faster than before. Thus, a fully configured 7 series FPGA design that exploits the fabric speed and incorporates several embedded circuits and systems can present power consumption challenges that must be managed.

Unlike features in an ASIC or a microprocessor, the combination of FPGA features used in a user application are not known to the component supplier. Therefore, it remains a challenge for Xilinx to predict the power requirements of a given FPGA when it leaves the factory. Accurate estimates are obtained when the board design takes shape. For this purpose, Xilinx offers and supports a suite of integrated device power analysis tools to help users quickly and accurately estimate their design power requirements. 7 series devices are supported similarly to previous FPGA products. The uncertainty of design power requirements makes it difficult to apply canned thermal solutions to fit all users. Therefore, Xilinx devices do not come with preset thermal solutions. The user's operating conditions dictate the appropriate solution.

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Table 5-1 shows the thermal resistance data for 7 series devices (grouped in the packages offered). The data includes junction-to-ambient in still air, junction-to-case, and junction-to-board data based on standard JEDEC four-layer measurements.

- Thermal data is available on the Xilinx website at:
  http://www.xilinx.com/cgi-bin/thermal/thermal.pl.
- Compact package thermal models for these products are available on the Xilinx support download center (under the Device Model tab) at:
  http://www.xilinx.com/support/download/index.htm

Table 5-1: **Thermal Resistance Data—All Devices**

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
Artix-7 FPGAs								
CP(G)236	10 x 10	XC7A8	41.0	23.4	8.89	35.2	33.3	32.0
		XC7A15	41.0	23.4	8.89	35.2	33.3	32.0
CS(G)225	12 x 12	XC7A30T	26.1	10.9	4.94	21.1	19.7	18.8
		XC7A50T	26.1	10.9	4.94	21.1	19.7	18.8
CS(G)324	15 x 15	XC7A8	29.6	16.1	7.41	24.6	23.2	22.4
		XC7A15	29.6	16.1	7.41	24.6	23.2	22.4
		XC7A30T	24.5	11.3	4.67	19.6	18.4	17.6
		XC7A50T	24.5	11.3	4.67	19.6	18.4	17.6
		XC7A100T	21.9	8.8	3.37	16.8	15.6	15.0
FT(G)256	17 x 17	XC7A8	31.2	21.1	11.08	26.5	25.0	24.2
		XC7A15	31.2	21.1	11.08	26.5	25.0	24.2
		XC7A30T	24.3	14.2	7.14	19.8	18.5	17.7
		XC7A50T	24.3	14.2	7.14	19.8	18.5	17.7
		XC7A100T	21.8	11.0	5.24	16.9	16.6	14.9
FB(G)484	23 x 23	XC7A200T	14.2	4.6	0.05	10.2	9.1	8.6
		XC7A350T	14.3	4.2	0.05	9.6	8.6	8.1
FG(G)484	23 x 23	XC7A30T	19.7	11.3	7.01	15.1	14.0	13.5
		XC7A50T	19.7	11.3	7.01	15.1	14.0	13.5
		XC7A100T	17.9	9.1	5.48	13.3	12.2	11.7
FB(G)676	27 x 27	XC7A200T	14.3	4.6	0.05	9.5	8.4	7.9
		XC7A350T	13.3	4.0	0.04	8.7	7.7	7.1
FG(G)676	27 x 27	XC7A100T	16.8	8.5	5.2	12.3	11.3	10.8
FF(G)1156	35 x 35	XC7A200T	10.2	3.7	0.33	6.4	5.4	4.8
		XC7A350T	9.8	2.2	0.23	6.1	5.2	4.6

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Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
Kintex-7 FPGAs								
FB(G)484	23 x 23	XC7K70T	16.4	6.6	0.16	12.0	11.0	10.4
		XC7K160T	13.5	5.0	0.06	10.4	9.4	8.8
FB(G)676	27 x 27	XC7K70T	15.8	6.8	0.16	11.7	10.8	10.2
		XC7K160T	12.8	5.1	0.09	9.8	8.9	8.3
		XC7K325T	11.8	4.0	0.04	9.1	8.1	7.5
		XC7K410T	11.1	3.6	0.03	8.5	7.5	7.0
FB(G)900	31 x 31	XC7K325T	11.3	4.1	0.04	8.8	7.9	7.3
		XC7K410T	10.6	4.3	0.04	8.3	7.3	6.8
FF(G)676	27 x 27	XC7K160T	10.5	4.4	0.41	7.4	6.4	5.8
		XC7K325T	9.5	3.7	0.25	7.1	6.1	5.6
		XC7K410T	9.3	3.4	0.19	6.8	5.9	5.4
FF(G)900	31 x 31	XC7K325T	8.4	2.6	0.24	6.1	5.3	5.0
		XC7K410T	8.2	2.6	0.19	5.9	5.1	4.7
FF(G)901	31 x 31	XC7K355T	8.6	3.6	0.22	6.1	5.3	4.8
		XC7K420T	8.1	3.2	0.19	6.0	5.2	4.7
		XC7K480T	7.6	3.2	0.17	5.9	5.1	4.6
FF(G)1156	35 x 35	XC7K420T	7.3	3.2	0.19	5.8	4.9	4.4
		XC7K480T	7.0	3.1	0.17	5.6	4.8	4.3
Virtex-7V FPGAs								
FF(G)1157	35 x 35	XC7V585T	6.9	2.2	0.13	5.4	4.6	4.3
FF(G)1761	42.5 x 42.5	XC7V585T	5.9	2.1	0.11	4.6	3.9	3.6
FL(G)1761	42.5 x 42.5	XC7V1500T						
FH(G)1761	42.5 x 42.5	XC7V2000T						
FL(G)1925	45 x 45	XC7V2000T						

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Table 5-1: **Thermal Resistance Data—All Devices *(Cont'd)***

Package	Package Body Size	Devices	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)	θ_{JA} (°C/W) @ 250 LFM	θ_{JA} (°C/W) @ 500 LFM	θ_{JA} (°C/W) @ 750 LFM
Virtex-7VX FPGAs								
FF(G)1157	35 x 35	XC7VX330T	7.4	2.3	0.18	5.6	4.8	4.4
		XC7VX415T	7.0	2.1	0.14	5.4	4.7	4.3
		XC7VX485T	6.7	2.4	0.11	5.3	4.6	4.2
		XC7VX690T	6.1	2.0	0.04	4.8	4.2	3.8
FF(G)1158	35 x 35	XC7VX415T	6.8	2.2	0.13	5.4	4.7	4.3
		XC7VX485T	6.4	2.2	0.11	5.2	4.6	4.2
		XC7VX550T	6.5	2.1	0.09	5.2	4.5	4.2
		XC7VX690T	6.2	2.1	0.04	4.8	4.2	3.8
FF(G)1761	42.5 x 42.5	XC7VX330T	6.4	2.3	0.19	4.8	4.1	3.7
		XC7VX485T	5.8	2.0	0.13	4.5	3.9	3.5
		XC7VX690T	5.4	1.9	0.09	4.3	3.7	3.4
FF(G)1926	45 x 45	XC7VX690T	4.9	1.8	0.07	4	3.5	3.1
		XC7VX980T	4.8	1.7	0.04	3.8	3.2	2.9
FF(G)1927	45 x 45	XC7VX415T	5.6	1.8	0.14	4.3	3.7	3.3
		XC7VX485T	5.2	1.8	0.13	4.5	3.8	3.4
		XC7VX550T	5.4	1.8	0.09	4.2	3.6	3.3
		XC7VX690T	4.9	1.8	0.07	3.8	3.2	2.9
FF(G)1928	45 x 45	XC7VX980T	4.8	1.7	0.04	4.0	3.4	3.1
FF(G)1930	45 x 45	XC7VX485T	5.5	1.8	0.11	4.3	3.6	3.3
		XC7VX690T	5.2	1.7	0.04	3.9	3.3	3.0
		XC7VX980T	5.0	1.7	0.04	3.8	3.2	2.9

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Power Management Strategy

Xilinx relies on a multi-prong approach with regards to the heat-dissipating potential of 7 series devices:

- Design and Silicon

  Significant power reduction in 7 series devices at the 28 nm node is achieved through innovative process and circuit design. For example, transistor static leakage current is minimized by more than 50 percent (comparable devices) by deploying multi-gate oxide transistors in the power-efficient 7 series architecture. Despite these improvements and a lower operating voltage, the base transistor counts are higher for these 7 series devices. They pack higher gate densities and the fabric is faster. Compared to previous generations, the power consumption is lower for the same design (same function and gate density) in a 7 series FPGA implementation.

  However, the increased resources and functionality associated with these higher gate density devices and faster switching fabric implies that more computation is possible in shorter time. Associated with this improved functionality is potential higher power dissipation that would have been worse without the silicon and device-based innovations.

- Packaging

  At the package component level, Xilinx has selected the more efficient flip-chip BGA packages, which present a low thermal path to the outside. This package incorporates a heat spreader with a thermal interface material (TIM), as shown in Figure 5-1.

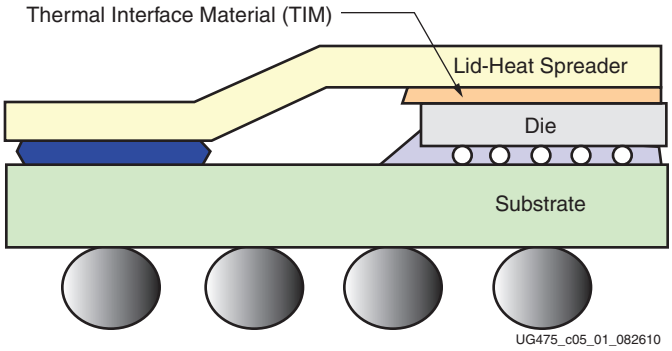

Figure 5-1: **Heat Spreader with Thermal Interface Material**

Materials with better thermal conductivity and consistent process applications deliver low thermal resistance up to the heat spreader. The junction-to-case thermal resistance (top of heat spreader) of all 7 series FPGA packages is typically less than 0.20°C/W. These packages deliver a low resistance platform for heat sink applications.

The parallel effort to ensure optimized package electrical return paths has produced an added benefit of enhanced power and ground plane arrangement in the packages. The boost in copper density on the planes improves the overall thermal conductivity through the laminate. In addition, the extra dense and distributed via fields in the package increase the vertical thermal conductivity. These packages offer up to 20% lower θ_{JB} compared to previous flip-chips packages.

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- Heat Sinking Solutions at the System Level

  Depending on the system's physical as well as mechanical constraints, the expectation is that the thermal budget is maintained with custom or OEM heat sink solutions, providing the third prong in the thermal management strategy. At this point, Xilinx has left the heat sink solution to the system-level designers who can tailor the design and solution to the constraints of their systems, being fully aware that the part has certain inherent capabilities for delivering the heat to the surface.

  Heat sink solutions do exist and can be effective on these low θ_{JB} flip-chip platforms. Table 5-2 illustrates a finned heat sink solution matrix in Network environment (1U and 2U) arrangement for 35 mm packages and up for power ranging from 15W to 40W. The AAVID standard finned heat sink offerings are used to illustrate the coverage given thermal budgets of ΔT = 35°C and ΔT = 45°C scenarios. Other heat sink configurations can be explored similarly.

Table 5-2: **Finned Heat Sink Solution Matrix for Large Flip-chip BGA in Network**

Package Power (W)		35 x 35 mm FF1156		42.5 x 42.5 mm FF1761	
		ΔT=35°C	ΔT=45°C	ΔT=35°C	ΔT=45°C
15W	1U(5)	Note 1		Note 1	
	2U(6)	Note 1		Note 1	
25W	1U(5)	Note 4	Note 2	Note 4	Note 2
	2U(6)	Note 2	Note 1	Note 2	Note 1
35W	1U(5)	Note 4	Note 3	Note 4	Note 3
	2U(6)	Note 4	Note 2	Note 4	Note 2
40W	1U(5)	–	–	Note 4	Note 3
	2U(6)	–	–	Note 3	Note 2

Notes:

1. Solution available at 200 LFM, for example, AAVID finned part number 68520, 72390, 72415.
2. Solution available at 400 LFM, for example, AAVID finned part number 68520, 69920.
3. Solution available at 600 LFM, for example, AAVID finned part number 72390, 69920, 74590.
4. No standard. AAVID finned solution below 600 LFM—custom finned might be required.
5. For 1U Height—(max heat sink height = 26 mm)
6. For 2U Height—(max heat sink height = 64 mm

The 7 series FPGA packages can be grouped into medium- and high-performance packages based on their power handling capabilities. All 7 series FPGA packages can use thermal enhancements, ranging from simple airflow to schemes that can include passive as well as active heat sinks. This is particularly true for the bigger flip-chip BGA packages where system designers have the option to further enhance the packages with bigger and more elaborate heat sinks to handle excesses of 25W with arrangements that consider system –physical constraints as illustrated in Table 5-2.

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Some Thermal Management Options

The flip-chip thermal management chart in Figure 5-2 illustrates simple but incremental power management schemes that can be applied on a flip-chip BGA package.

Low End 1–6W	Bare Package with Moderate Air 8–12°C/W	Bare Package Package can be used with moderate airflow within a system
Mid Range 4–10W	Passive H/S + Air 5–10°C/W	Packaged Used with Various Forms of Passive Heat Sinks Heat spreader techniques
High End 8–25W	Active Heat Sink 2–3°C/W or Better	Package Used with Active Heat Sinks TEC and board level heat spreader techniques

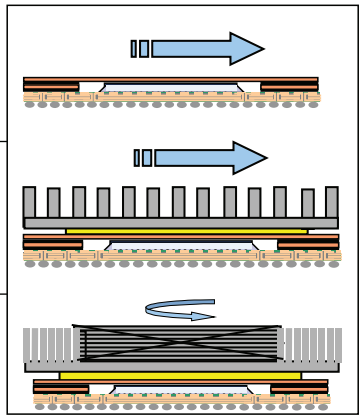

Figure 5-2: **Thermal Management Options for Flip-Chip BGA Packages**

- For moderate power dissipation (less than 6W), the use of passive heat sinks and heat spreaders attached with thermally conductive double-sided tapes or retainers (with TIM around 0.2°C/W) can offer quick thermal solutions in these packages.
- The use of lightweight, finned, external, passive heat sinks can be effective for dissipating up to 10–25W in the bigger packages. The more efficient external heat sinks tend to be tall and heavy. To help protect component joints from heat sink induced stress cracks, the use of spring-loaded pins or clips that transfer the mounting stress to a circuit board is advisable whenever a bulky heat sink is considered.
- As stated earlier, the flip-chip BGA packages offered for 7 series devices are thermally enhanced BGAs with the die facing down. These packages have an exposed metal heat sink at the top. These high-end thermal packages lend themselves to the application of efficient external heat sinks (passive or active) for further heat removal efficiency. Again, precautions must be taken to prevent component damage when a bulky heat sink is attached. The thermal interface resistance needs to be controlled to take full advantage of these packages.
- An active heat sink might include a simple heat sink incorporating a mini fan or even a Peltier Thermoelectric Cooler (TEC) with a fan to carry away any dissipated heat. When considering the use of a TEC for heat management, consultation with experts in using the device is important because these devices can be reversed and cause damage to components. Also condensation can be an issue with these devices.
- The printed circuit board on which the package is mounted can have a significant impact on thermal performance. As much as 60 to 80 percent of the dissipated heat can go through the BGA balls and thus to the board. A typical systems board is larger than the standard 4 x 4 in JEDEC thermal board. Components mounted on these boards with multiple copper layers and several internal vias show low effective junction-to-ambient thermal resistances.

  Table 5-3 shows this impact as an FF1156 flip-chip package's effective junction to ambient resistance is changed depending on the mounting board.

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Table 5-3: **Impact of Mounted Board Characteristics on θ_{JA}(FF1156)**

Xilinx 35 x 35mm FF1156		θ_{JA} (°C/W) for Different Board Sizes		
		4 x 4 in	10 x 10 in	20 x 20 in
Layer Count of Mounted Board	4	9.1 (1)	8.3	–
	8	8.0	5.5	4.9
	12	7.5	4.7	4.4
	16	7.2	4.5	4.2
	24	–	4.3	4.0

Notes:

1. Base JEDEC Mount Conditions

- Designs can be implemented to take advantage of the board's ability to spread heat. The effect of the board is dependent on its size and how it conducts heat. Board size, the level of copper traces, and the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package mounted on the board. The cold ring junction-to-board thermal data for 7 series FPGA packages are given in Table 5-1. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources on the board, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat contributing components on the board.

Support for Compact Thermal Models (CTM)

Table 5-1 provides the traditional thermal resistance data for 7 series devices. These resistances are measured using a prescribed JEDEC standard that might not necessarily reflect the user's actual board conditions and environment. The quoted θ_{JA} and θ_{JC} numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system-level thermal simulation might be required. Though Xilinx continues to support these figure of merit data, for 7 series FPGAs, boundary conditions independent compact thermal models (BCI-CTM) are also available to assist users in their thermal simulations.

Two-resistor as well as eight to ten-resistor network models are offered for all 7 series devices. These compact models seek to capture the thermal behavior of the packages more accurately at predetermined critical points (junction, case, top, leads, and so on) with the reduced set of nodes as illustrated in Figure 5-3.

Unlike a full 3D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTM models are available on the Xilinx support download center (under the Device Model tab) at:

http://www.xilinx.com/support/download/index.htm

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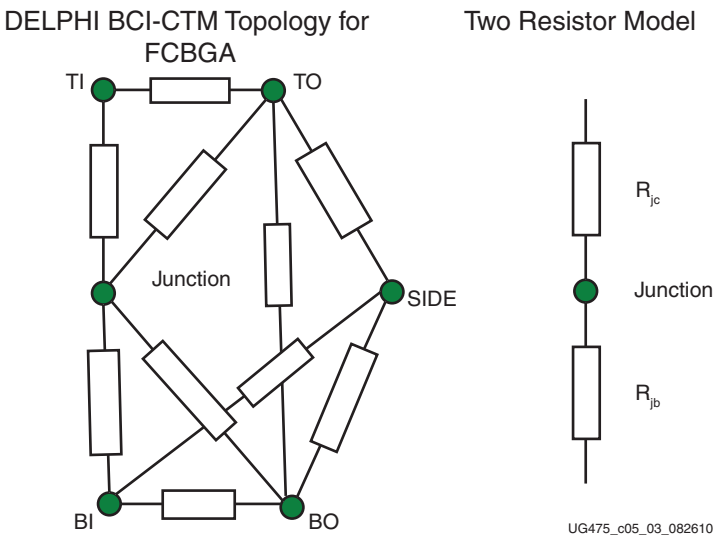

Figure 5-3: **Thermal Model Topologies**

The CTM models are based on the DELPHI approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the DELPHI approach is used to generate these files and the data saved in the NATIVE and proprietary file formats of the targeted CFD tools - rather than follow a neutral file format. The CTM libraries are available in Flotherm (PDML) format – good for V5.1 and above and Icepack (version 4.2 and above) format.

References

The following websites contain additional information on heat management and contact information.

- http://www.wakefield.com
- http://www.aavidthermalloy.com
- http://www.qats.com

Refer to the following websites for interface material sources:

- Power Devices - http://www.powerdevices.com
- Bergquist Company - http://www.bergquistcompany.com
- AOS Thermal Compound - http://www.aosco.com
- Chometrics - http://www.chomerics.com
- Kester - http://www.kester.com

Refer to the following websites for CFD tools Xilinx supports with thermal models.

- Flomerics - Flotherm & FloPCB - http://www.flomerics.com
- Fluent - Icepak - http://www.icepak.com

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Chapter 6

Package Marking

All 7 series devices have package top-markings similar to the examples shown in Figure 6-1 and Figure 6-2 and explained in Table 6-1.

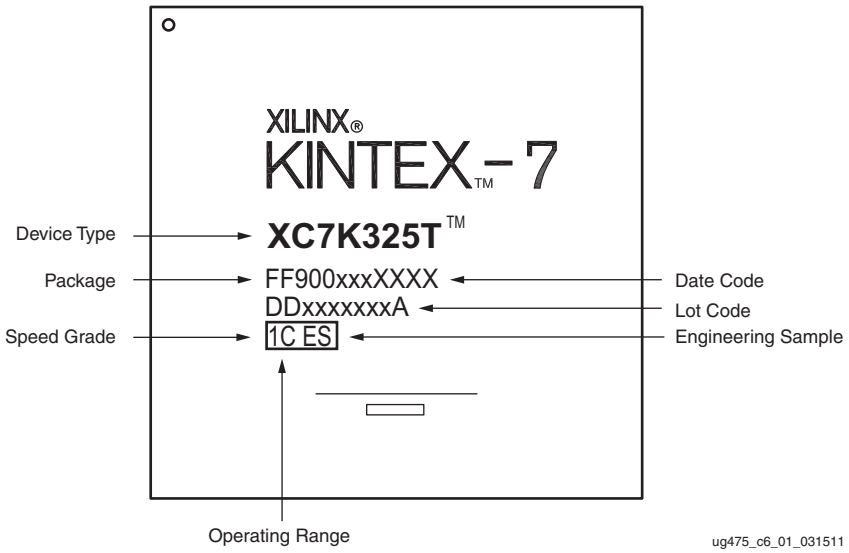

Figure 6-1: **Kintex-7 Device Package Marking**

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Figure 6-2: **Virtex-7 Device Package Marking**

Table 6-1: **Xilinx Device Marking Definition—Example**

Item	Definition	
Xilinx Logo	Xilinx logo, Xilinx name with trademark, and trademark-registered status.	
Family Brand Logo	Device family name with trademark and trademark-registered status. This line is optional and could appear blank.	
1st Line	Device type.	
2nd Line	Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code. A *G* in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: http://www.xilinx.com/pbfree.	
3rd Line	Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist.	
4th Line	Device speed grade and temperature range. When not marked on the package, the product is considered to operate at the commercial (C) temperature range. For more information on the ordering codes, see DS180: *7 Series FPGAs Overview*. Other variations for the 4th line:	
	L2E	The *L2E* indicates a -2LE device. The -2L devices operate at either of two voltages, 0.9V and 1.0V. The E is for the extended temperature operating range. For more information, see the specific device's data sheet at: http://www.xilinx.com/support/documentation/7_series.htm#156339.
	1C xxxx	The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark.
	1C ES	The *ES* indicates an Engineering Sample.

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Appendix A

Recommended PCB Design Rules for BGA Packages

Xilinx provides the diameter of a land pad on the component side. This information is required prior to the start of the board layout so the board pads can be designed to match the component-side land geometry. The typical values of these land pads are described in Figure A-1 and summarized in Table A-1. For Xilinx® BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested to allow a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure A-1. The space between the NSMD pad and the solder mask as well as the actual signal trace widths depend on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

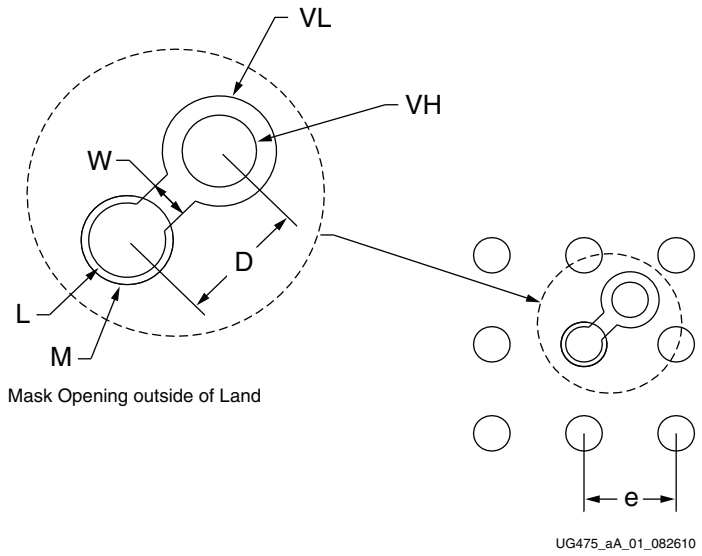

Figure A-1: **Suggested Board Layout of Soldered Pads for BGA Packages**

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Table A-1: **Recommended PCB Design Rules for All FF(G) Packages**

Design Rule	FF(G) Packages (Dimensions in mm)
Component Land Pad Diameter (SMD)(1)	0.53
Solder Land (L) Diameter	0.45
Opening in Solder Mask (M) Diameter	0.55
Solder (Ball) Land Pitch (e)	1.00
Line Width Between Via and Land (w)	0.13
Distance Between Via and Land (D)	0.70
Via Land (VL) Diameter	0.61
Through Hole (VH) Diameter	0.300

Notes:

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).

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