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Operating the ADG12xx Series of Parts with ±5 V Supplies and the Impact on Performance

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INTRODUCTION

Industrial design engineers require analog switches and multiplexers to support faster sampling, increased performance, lower power dissipation, and a smaller footprint. To meet these requirements, a range of low capacitance, low leakage, and low charge injection analog switches and multiplexers are required.

Analog Devices, Inc. *i*CMOS® process technology has enabled the introduction of a wide range of high performance switch and multiplexer solutions. The ADG12xx family of parts offers the industry's lowest capacitance, charge injection, and leakage for high end data acquisition in very small packages. These parts are fully specified with bipolar ±15 V supplies and +12 V single-supply operation.

The ADG12xx family of parts can also be operated with ±5 V supplies. This application note uses the key specifications of the ADG12xx and explains how these parts perform with the lower supply voltage. It also shows that advantage can still be taken of the high performance capacitance and charge injection offered by these parts even if only ±5 V supply voltages are available in the application.

The full list of ADG12xx parts are listed in Table 1. Complete specifications for each part with ±15 V/+12 V supplies can be found in the datasheets available from Analog Devices and should be consulted in conjunction with this application note.

Table 1. Key Specifications for the ADG12xx Series

Part No.	Function	On Capacitance (pF)	Q_{INJ} (pC)	R_{ON} (Ω)	On Leakage (pA)	Package
ADG1201	1 × SPST	2.6	−0.3	120	20	6-Lead SOT-23
ADG1202	1 × SPST	2.6	−0.3	120	20	6-Lead SOT-23
ADG1221	2 × SPST	2.6	−0.3	120	20	10-Lead MSOP
ADG1222	2 × SPST	2.6	−0.3	120	20	10-Lead MSOP
ADG1223	2 × SPST	2.6	−0.3	120	20	10-Lead MSOP
ADG1211	4 × SPST	2.6	−0.3	120	20	16-Lead TSSOP; 16-Lead, 3 mm × 3 mm LFCSP
ADG1212	4 × SPST	2.6	−0.3	120	20	16-Lead TSSOP; 16-Lead, 3 mm × 3 mm LFCSP
ADG1213	4 × SPST	2.6	−0.3	120	20	16-Lead TSSOP; 16-Lead, 3 mm × 3 mm LFCSP
ADG1219	1 × SPDT	3.5	−0.3	120	20	8-Lead SOT-23
ADG1236	2 × SPDT	3.5	−1	120	20	16-Lead TSSOP; 12-Lead, 3 mm × 3 mm LFCSP
ADG1233	3 × SPDT	3.5	+0.5	120	20	16-Lead TSSOP; 16-Lead, 4 mm × 4 mm LFCSP
ADG1234	4 × SPDT	3.5	+0.5	120	20	20-Lead TSSOP; 20-Lead, 4 mm × 4 mm LFCSP
ADG1204	4:1 mux	5.5	−0.7	120	20	14-Lead TSSOP; 12-Lead, 3 mm × 3 mm LFCSP
ADG1208	8:1 mux	6	+0.4	120	20	16-Lead TSSOP; 16-Lead, SOIC; and 16-Lead, 4 mm × 4 mm LFCSP
ADG1206	16:1 mux	11	+0.5	120	80	28-Lead TSSOP; 32-Lead, 5 mm × 5 mm LFCSP
ADG1209	Differential 4:1 mux	3.5	+0.4	120	20	16-Lead TSSOP; 16-Lead, SOIC; and 16-Lead, 4 mm × 4 mm LFCSP
ADG1207	Differential 8:1 mux	7	+0.5	120	80	28-Lead TSSOP; 32-Lead, 5 mm × 5 mm LFCSP

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±5 V PERFORMANCE

The ADG12xx family of switches and multiplexers are designed on Analog Devices, 33 V, *i*CMOS process technology for ±16.5 V maximum operating voltage. Therefore, the performance parameters are optimized at these higher supply voltages.

The main performance parameters affected with lower supply voltages on switches and multiplexers are the on resistance and timing. If low on resistance is a key performance requirement at ±5 V, then the Analog Devices families of ADG6xx and ADG14xx should be considered. The remainder of this application note outlines the level of performance expected at ±5 V on the ADG12xx series.

CAPACITANCE

The *i*CMOS process technology offers a significant reduction in parasitic capacitance per unit area. The design of the ADG12xx family is optimized for capacitance performance; thus, the die area has been kept to a minimum. This ensures very low parasitic capacitance because capacitance is largely dependent on the switch area. Efforts are also made during the layout of the device to minimize parasitic capacitance.

Capacitance is an important parameter to consider in any design and, therefore, the following parameters are specified in the data sheet:

C_S (Off)
The source off capacitance is measured between the source input and GND when the switch is off or disabled.

C_D (Off)
The drain off capacitance is measured between the drain output and GND when the switch is disabled.

C_D, C_S (On)
The on switch capacitance is measured between the input or output and GND. On capacitance is a measure of the source capacitance, drain capacitance, and the switch capacitance for an on switch.

C_{IN}

Digital input capacitance is the capacitance measured between digital input and GND.

Given that capacitance is mainly dependent on the process and die area, the operating voltage does not have a significant impact on performance levels. The very low capacitance featured at ±15 V is maintained when operating the part with ±5 V supplies. Figure 1 shows the capacitance performance of the ADG1206, 16:1 multiplexer with ±5 V supplies.

The drain on and drain off capacitance is a function of the number of switch channels connected to it. Therefore, the drain capacitance for an 8:1 multiplexer is typically half that of a 16:1 multiplexer.

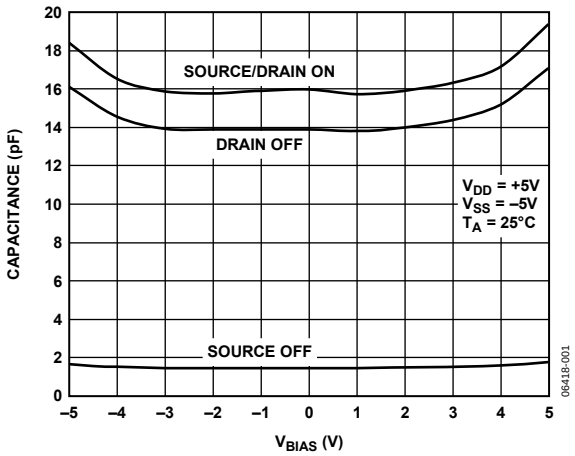

Figure 1. ADG1206 Capacitance at ±5 V Dual Supply

AC PARAMETERS

The very low parasitic capacitance of these parts ensures that these parts have excellent bandwidth, off isolation, and crosstalk performance. Capacitance and, consequently, the ac performance over frequency is not affected by lower supply voltages. Figure 2 through Figure 4 show the frequency performance of the ADG1204 part with ±5 V supplies. All measurements are taken with a 50 Ω, 5 pF output load.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch. Figure 2 shows that the off isolation at 1 MHz is −85 dB typically with a ±5 V supply on the ADG1204.

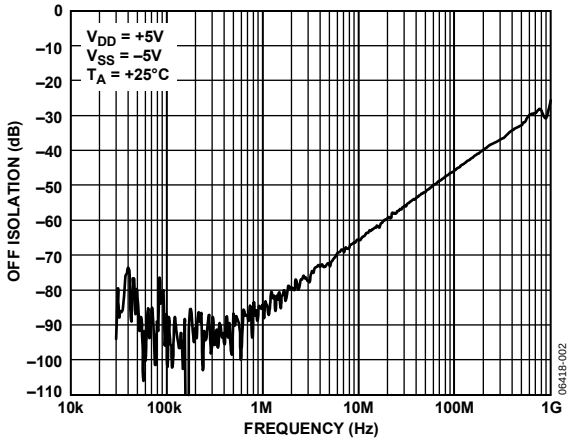

Figure 2. ADG1204 Off Isolation vs. Frequency

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance. Figure 3 shows that the adjacent channel crosstalk at 1 MHz is −80 dB typically with ±5 V supply on the ADG1204.

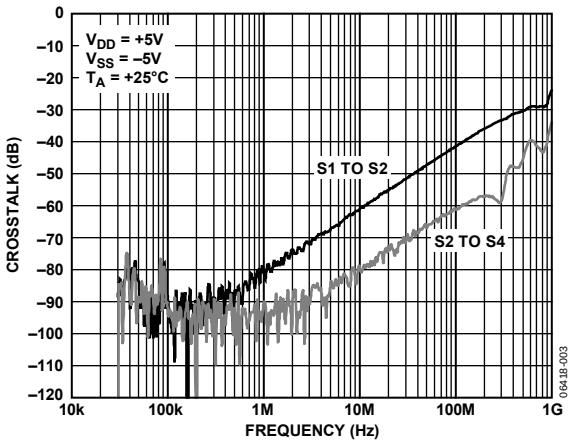

Figure 3. ADG1204 Crosstalk vs. Frequency

Bandwidth

Bandwidth is the frequency at which the output is attenuated by −3 dB. With ±5 V supplies, the ADG1204 −3 dB point is 600 MHz. The insertion loss deteriorates with lower supply voltage due to the increase in on resistance performance. Figure 4 shows the frequency response when the switch is on for the ADG1204.

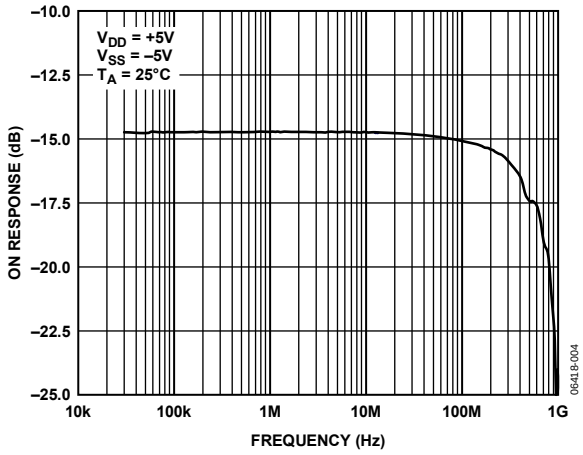

Figure 4. ADG1204 On Response vs. Frequency

CHARGE INJECTION

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching. It is caused by stray capacitance associated with the NMOS and PMOS transistors that make up the analog switch. In switch applications, charge injection introduces gain error and dc offset errors thereby impacting the overall system accuracy.

The ADG12xx parts have excellent charge injection performance due to the lower parasitic capacitance on the *i*CMOS process and better matching of the NMOS and PMOS transistors. The ADG1211, ADG1212, ADG1213, ADG1236, ADG1233, ADG1234, and the ADG1204 charge injection performance is typically ±1 pC over the full signal with ±5 V power supplies. See Figure 5 for a typical performance curve.

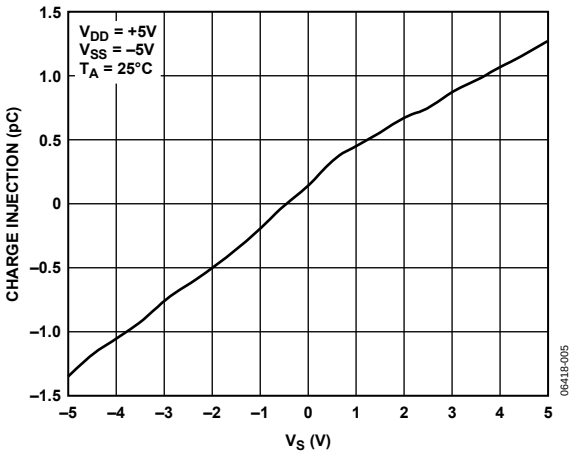

Figure 5. Charge Injection vs. Source Voltage

The design techniques used for the ADG1208, ADG1209, ADG1206, and ADG1207 multiplexers mean that the charge injection performance is virtually flat over the full signal range. This is achieved by placing a compensation switch on the drain of the multiplexers. Figure 6 shows the performance of the ADG1208, ADG1209, ADG1206, and ADG1207 when used as a multiplexer (source-to-drain) at ±5 V supplies. The charge injection is typically 0.15 pC and there is minimal variation over input signal. The demultiplexer (drain-to-source) charge injection performance is typically that as shown in Figure 5. This makes these multiplexers ideal in any application that demands minimized charge injection, for example, in sample-and-hold systems.

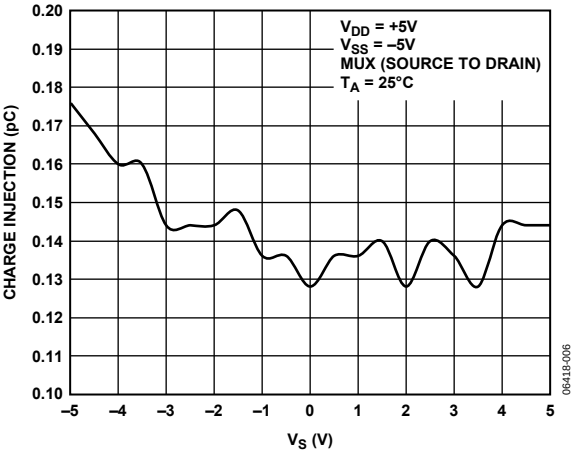

Figure 6. Source-to-Drain Charge Injection vs. Source Voltage

TRIGGER LEVELS

The input buffer on the ADG12xx parts is powered from GND and V_{DD}. The ADG12xx parts have 3 V logic-compatible inputs with V_{IH} = 2 V minimum and V_{IL} = 0.8 V maximum. These levels are fully guaranteed in the data sheets at ±15 V and +12 V. There is very little variation in the trigger point with varying supply for both dual-supply (see Figure 7) and single-supply operation (see Figure 8).

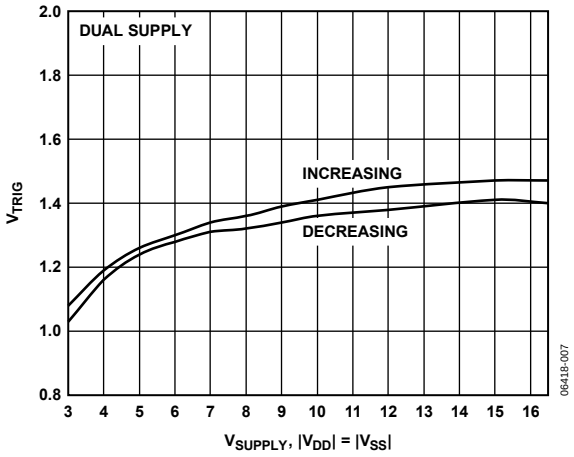

Figure 7. Trigger Level as a Function of Dual-Supply Voltage

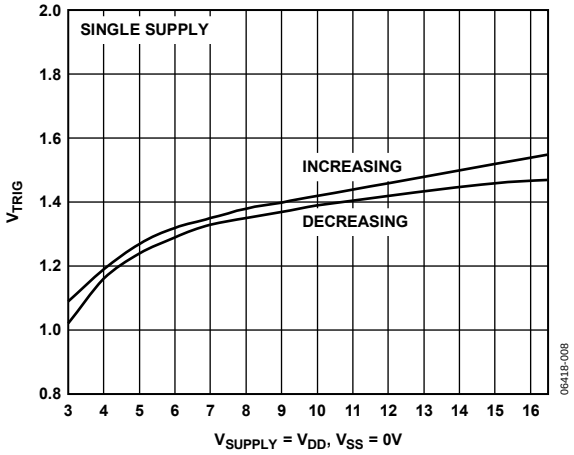

Figure 8. Trigger Level as a Function of Single-Supply Voltage

ON RESISTANCE

The on resistance (R_{ON}) of a switch is a measure of the resistance between the input and the output. A signal passing through a switch suffers an IR drop, where R is a measure of the R_{ON} and I is the current.

The ADG12xx parts are optimized for low capacitance performance; therefore, the die area is kept to a minimum. However, when designing low R_{ON} switches, the die area is maximized to ensure low on resistance. Therefore, there is an obvious direct trade-off between capacitance and on resistance performance for switches and multiplexers.

Supply voltage has a significant impact on the on resistance performance of a switch. To obtain the lowest possible on resistance performance from switches and multiplexers, they should be operated with the maximum allowable operating voltage. This is ±16.5 V on the ADG12xx parts. Operating the part with a higher supply voltage also ensures less variation of input resistance with varying input signal. This dependence of operating voltage on the on resistance performance is clearly shown in Figure 9.

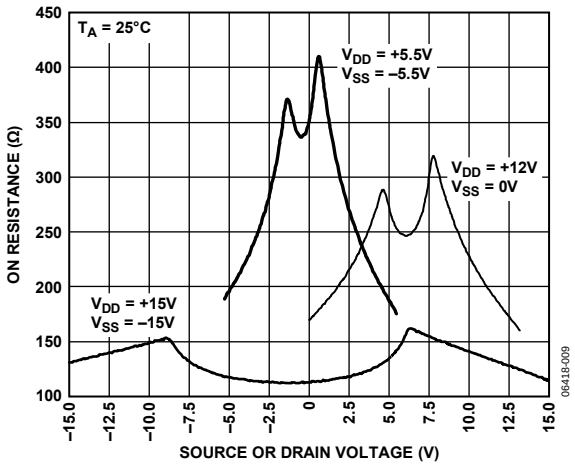

Figure 9. On Resistance as a Function of V_D (V_S) for Different Supply Voltages

The ADG12xx on resistance performance with ±5 V supplies is shown in Figure 10. This plot shows the on resistance performance at 5 V supplies and the performance with a 10% tolerance on these supplies. The same basic switch cells are used in the design of all the ADG12xx parts, making these on resistance plots typical of all configurations.

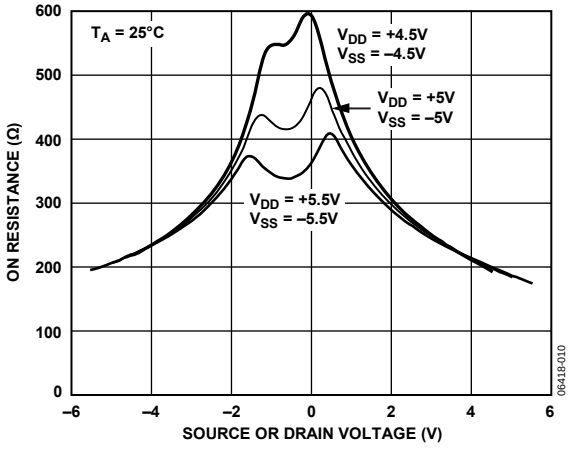

Figure 10. On Resistance as a Function of V_D (V_S)

As demonstrated in Figure 9 and Figure 10, the on resistance performance of switches and multiplexers is a function of supply and input signal. The on resistance performance also varies with temperature. How the on resistance varies with temperature at ±5 V supplies for the ADG1211, ADG1212, and

ADG1213 is shown in Figure 11. It is evident that the on resistance is higher with higher temperature.

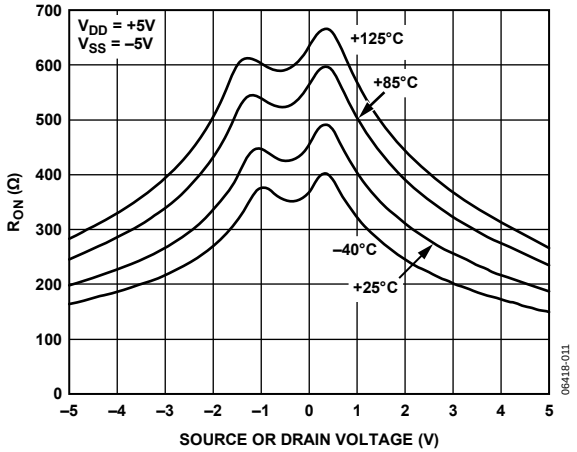

Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures

LEAKAGE

The *i*CMOS process technology and the design of the ADG12xx switches and multiplexers offer very low leakage performance. The leakage is typically around 20 pA.

I_S (Off)
Source leakage current when the switch is off.

I_D (Off)
Drain leakage current when the switch is off.

I_D, I_S (On)
Channel leakage current when the switch is on.

Figure 12 shows the leakage performance at a ±5 V supply for the ADG1206 16:1 multiplexer. The on leakage and drain off leakage are a function of the number of channels connected to the drain. This result, then, is a multiple of the number of channels.

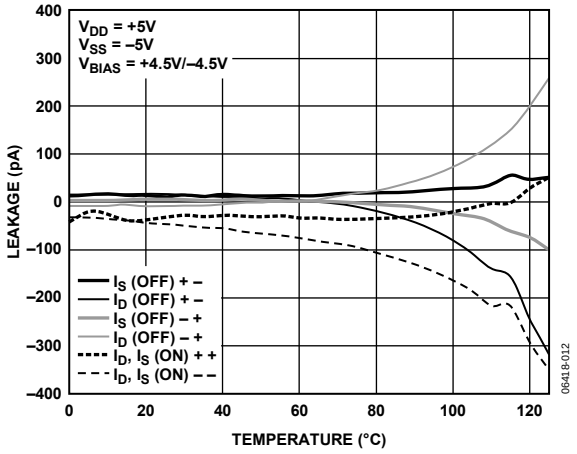

Figure 12. Leakage Currents as a Function of Temperature, Dual Supply

TIMING

The following timing parameters are the most commonly specified in the part data sheets for on switches and multiplexers.

t_{ON} ($\overline{EN}$)

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Break-before-make timing—off time measured between the 80% point of both switches when switching from one address state to another.

Timing performance is a function of temperature and supply voltage. Timing is slower with higher temperature and is slower with lower supply voltages. The Figure 13 shows the timing performance over temperature and supply voltage for the ADG1211, ADG1212, and ADG1213 quad SPST switches. It is evident that the typical t_{ON} time at ±5 V, 25°C is 225 ns and the typical t_{OFF} time is 110 ns.

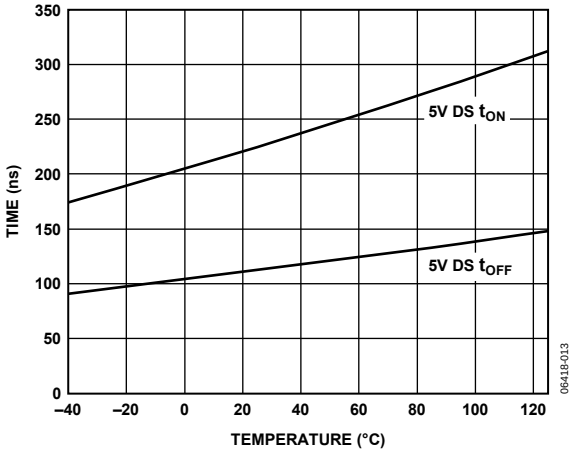

Figure 13. t_{ON}/t_{OFF} Time vs. Temperature at 5 V Dual Supply

CONCLUSION

The ADG12xx family of parts offer the industry's lowest capacitance, charge injection, and leakage for high end data acquisition in very small packages for ±15 V/+12 V systems. With lower supply voltages, the excellent capacitance, charge injection and leakage performance is maintained. The disadvantage of using the ADG12xx parts with ±5V supplies is a significant decrease to the on resistance and timing performance.

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