EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0182 Circuit Evaluation Board (EVAL-CN0182-SDZ)
System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a single-supply, low power, window detector with programmable upper and lower limits. This type of circuit can be used to generate an alarm if a signal falls outside the preset limits and is popular in detection and monitoring applications. The AD5668-1 octal, low power, 16-bit, buffered voltage-output DAC is used to set the limits of the window. The AD5668-1 has an on-chip, 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 0 V to 2.5 V. The internal reference is enabled using a software write. An SPI interface is used to communicate with the AD5668-1.

The comparator used is an ADCMP370, a general-purpose, low power comparator (20 µW typical at 5 V) with an input offset voltage of 9 mV maximum and an open-drain output.

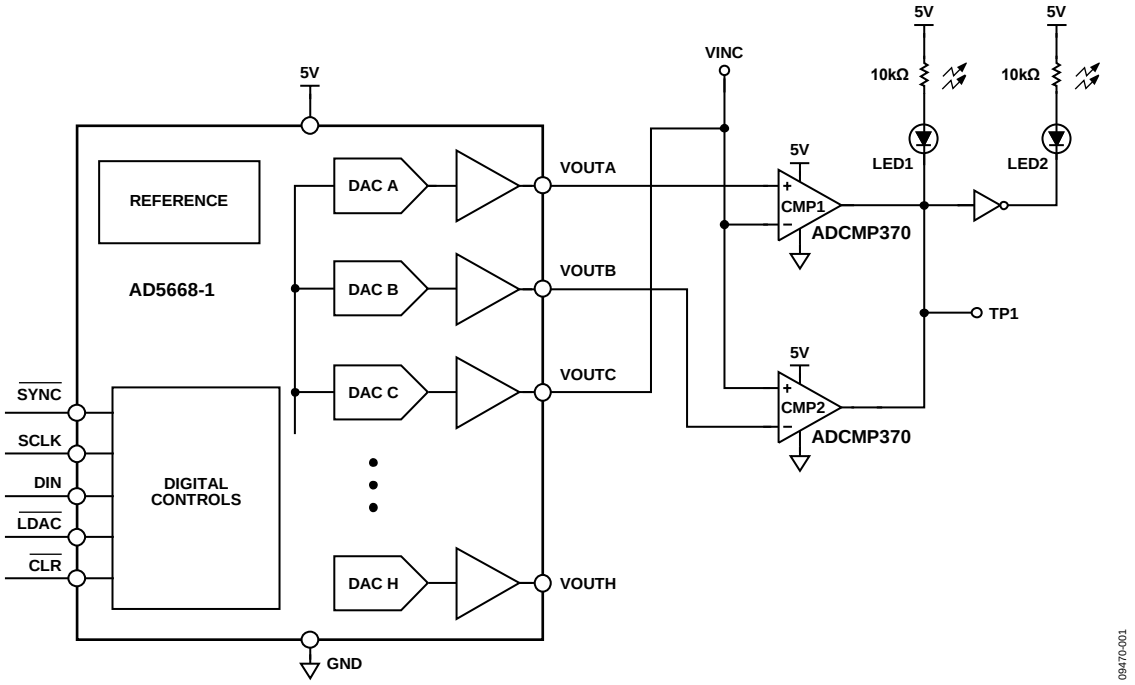

Figure 1. Low Power, Single-Supply Window Detector (Simplified Schematic: All Connections and Decoupling Not Shown)

CIRCUIT DESCRIPTION

The circuit in Figure 1 is an upper and lower limit programmable window detector. The upper and lower limits are loaded into each DAC register individually. The primary application of the circuit is to test if an external signal falls within the programmed limits.

The AD5668-1 is an octal DAC, and the outputs on Channel A and Channel B set the upper and lower limits, respectively.

For test purposes, DAC C provides the signal input. When the signal enters the region set by DAC A and DAC B, the voltage at TP1 goes to Logic 1, LED1 is off, and LED2 is on. When the signal is outside the window set by the upper and lower limits, LED1 is on, and LED2 is off.

If a pull-up resistor is connected to the output of the ADCMP370, its output is 5 V if the noninverting input is greater than the inverting input; otherwise, it is 0 V.

The ADCMP370 has an open-drain output, allowing the output of Comparator C1 and Comparator C2 to be wire-AND'ed together. The truth table for the circuit is shown in Table 1. In this example, VOUTA is the upper limit, VOUTB is the lower limit, and VOUTA > VOUTB.

The circuit operation is illustrated in Figure 2. DAC C generates a 0 V to 2.5 V triangle waveform that drives the VINC (TP2/TESTC) input to the comparators. The threshold levels are set by DAC A (VOUTA = 2 V) and DAC B (VOUTB = 1 V). The voltage at TP1 goes to a Logic 1 when the VINC voltage is between the two thresholds.

Table 1. Truth Table of Circuit

VINC Level	Output CMP1	Output CMP2	Output CMP1 AND Output CMP2	TP1	LED1	LED2
VINC < VOUTB < VOUTA	1	0	0	0	On	Off
VINC > VOUTA > VOUTB	0	1	0	0	On	Off
VOUTB < VINC < VOUTA	1	1	1	1	Off	On

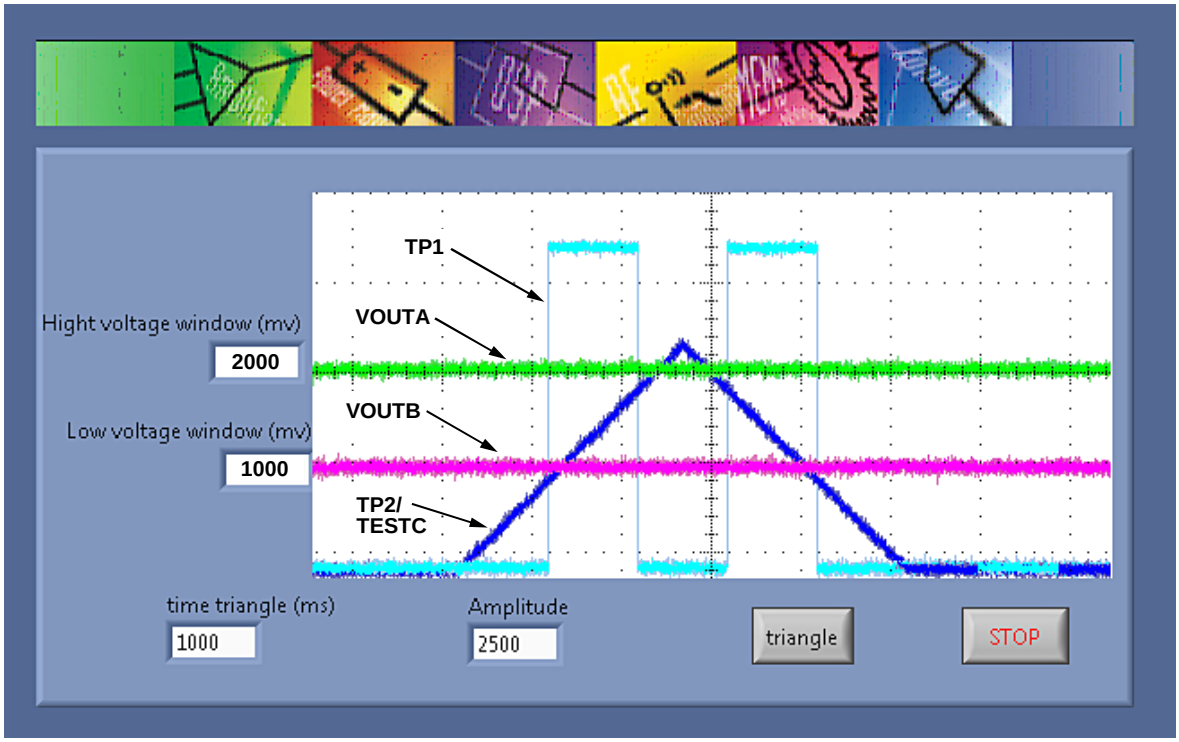

Figure 2. Output of Window Comparator for VOUTA = 2 V, VOUTB = 1 V, and VINC = Ramp from 0 V to 2.5 V

COMMON VARIATIONS

The AD5668-2 and AD5668-3 have a 2.5 V, 5 ppm/°C reference, giving a full-scale output range of 0 V to 5 V.

The AD5668-1 and AD5668-2 have a power-on-reset circuit that powers up to 0 V until a valid write takes place. The AD5668-3 powers up to midscale.

CIRCUIT EVALUATION AND TEST

Equipment Needed (Equivalents Can Be Substituted)

- EVAL-SDP-CB1Z System Demonstration Platform
- CN-0182 Circuit Evaluation Board (EVAL-CN0182-SDZ)
- CN-0182 Evaluation Software
- Tektronix TDS2024, 4-channel oscilloscope
- HP-E3630A, 0 V to 6 V, 2.55 A ± 20 V, 0.5 A triple output dc power supply
- PC (Windows® 32-bit or 64-bit)

Getting Started

Load the evaluation software by placing the CN-0182 evaluation software CD in the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software CD and open the **Readme** file.

Follow the instructions contained in the **Readme** file for installing and using the evaluation software.

Functional Block Diagram

Figure 3 shows a functional diagram block of the test setup.

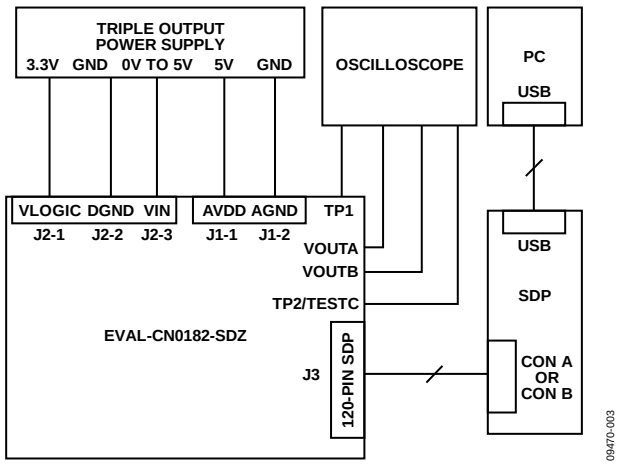

Figure 3. Test Setup Functional Block Diagram

Setup

Connect the 120-pin connector on the EVAL-CN0182-SDZ circuit board to the CON A or CON B connectors on the EVAL-SDP-CB1Z evaluation (SDP) board. Use screws to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. After successfully setting the dc output supply to 5 V and 3.3 V, turn the power supply off.

With the power supply off, connect the 5 V power supply to the J1-1 pin (AVDD), connect GND to the J1-2 and J2-2 pins, respectively (AGND and DGND), connect 3.3 V to the J2-1 pin (VLOGIC). Alternatively, place Link 2 in Position B to power the digital circuitry from the USB port via the SDP board (default setting). VLOGIC is not needed in this case.

Turn on the power supply and then connect the USB cable with the SDP board to the USB port on the PC. Note: do not connect the USB cable to the mini-USB connector on the SDP board before turning on the dc power supply for the EVAL-CN0182-SDZ.

Test

After setting up the test equipment, connect the probes of the oscilloscope to the test points marked TP1, VOUTA, VOUTB, and TP2/TESTC.

The provided software allows the value of VOUTA and VOUTB to be set, defining the window. If the default settings are kept, press **triangle** in the main software window to create a triangle signal on VINC, as shown in Figure 2. The duration and the amplitude of this signal can be varied. This signal can be observed on the TP2/TESTC test point. With a 1 second duration, and VOUTA and VOUTB settled to 2000 mV and 1000 mV, respectively, the two LEDs blink as the value of VINC comes in and out of the limits, as explained in the Circuit Description section. The AD5668-1 DAC limits the maximum value for VOUTA, VOUTB, and VINC at 2.5 V.

Putting Link 5 in Position A allows the external signal, VINC, to be applied on the VIN pin. This can be observed on the TP2 test point. In addition, the output can be observed on the TP1 test point.

When Link 1 is not inserted, the output changes depending on the level of VINC compared to VOUTA.

Table 2. Jumper Settings (Default Settings Bolded Within Table)

Jumper	Description	Setting	Function
LK1	CMP1 and CMP2 comparator output connections	**Inserted**	**The CMP1 and CMP2 outputs are shorted together at TP1. This is the window comparator configuration.**
		Opened	The two CMP outputs are not shorted. CMP1 is linked to the LEDs only, and VINC is only compared to VOUTA (high level).
LK2	Digital supply source	Position A	The digital circuit is supply by an external power supply connected to the J2-1 pin (VLOGIC).
		Position B	**The digital power is supply by the SDP board; it is not necessary to put any voltage on the VLOGIC pin.**
LK5	VINC voltage source	**Position A**	**VINC is set by the SDP and can be measured on the TESTC test point.**
		Position B	VINC is set by an external supply (0 V to 5 V) through the J2-3 pin (VIN) and can be measured on the TP2 test point.

LEARN MORE

CN-0182 Design Support Package:
http://www.analog.com/CN0182-DesignSupport

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

CN-0182 Circuit Evaluation Board (EVAL-CN0182-SDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

AD5668 Data Sheet and Evaluation Board

ADCMP370 Data Sheet and Evaluation Board

REVISION HISTORY

4/12—Rev. 0: Initial Version