EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

CN-0183 Circuit Evaluation Board (EVAL-CN0183-SDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 provides a precision 16-bit, low drift bipolar voltage output of ±2.5 V and operates on a single +10 V to +15 V supply. The unipolar voltage outputs of the AD5668 octal *dense*DAC are amplified and level shifted by the AD8638 auto-zero op amps. The maximum drift contribution of the AD8638 is only 0.06 ppm/°C. The external REF192 reference ensures a maximum drift of 5 ppm/°C (E grade) and provides a low impedance pseudo ground for the AD8638 level gain and shifting circuit.

The circuit offers an efficient solution to a problem often encountered in systems with a single +12 V supply rail. Proper printed circuit board (PCB) layout and grounding techniques ensure that the ADP2300 switching regulator does not degrade the overall performance of the circuit.

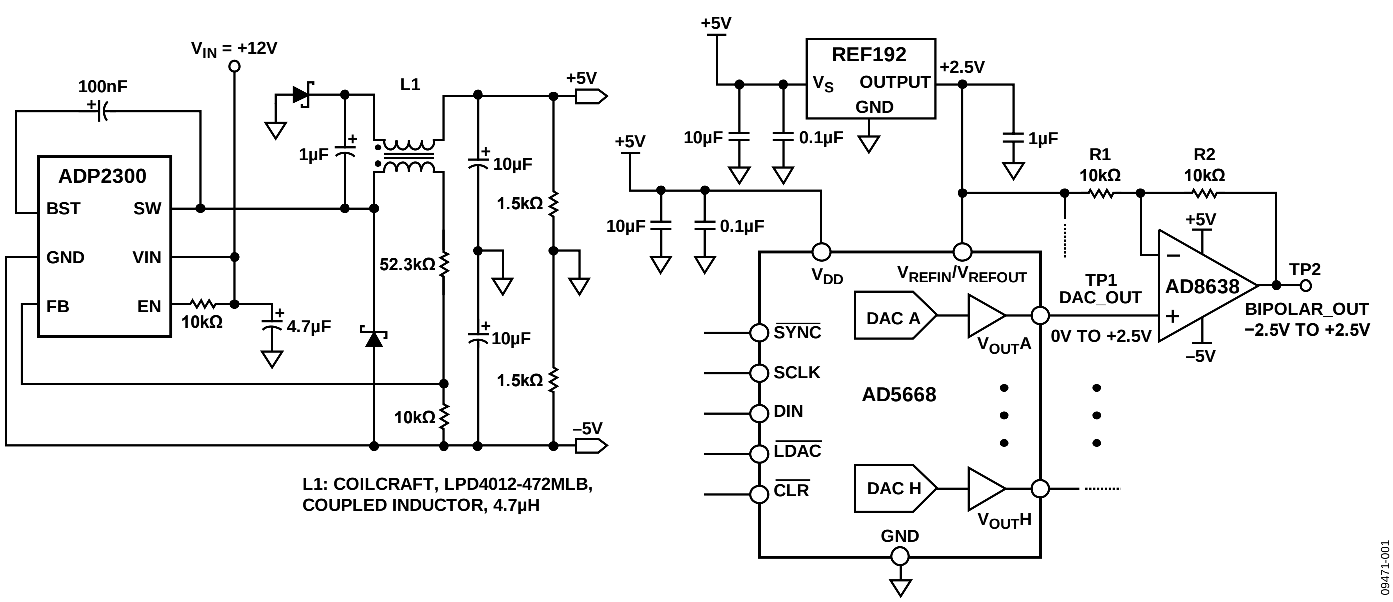

Figure 1. Bipolar Output DAC Circuit with ±5 V Power Supplies

CIRCUIT DESCRIPTION

The AD5668 is a 16-bit, octal, voltage output *dense*DAC controlled by an SPI interface. It contains an on-chip reference with a 10 ppm/°C maximum drift specification. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. In the circuit shown in Figure 1, an external REF192 is used because a low output impedance is required to drive the 2.5 V pseudo ground reference for the AD8638 op amps.

The output voltage of the AD5668 is 0 V to 2.5 V at TP1, and this signal drives the noninverting input of the AD8638 op amp. The signal gain of the op amp is 1 + R2/R1, which is 2 for R1 = R2. A negative 2.5 V offset is injected into the op amp output by driving R1 with the 2.5 V reference. The result is a bipolar output voltage at TP2 that swings from −2.5 V to +2.5 V.

The circuit operates on a single supply voltage of nominally 12 V, which can vary between 10 V and 15 V. The regulated −5 V supply rail is developed from an ADP2300 switching regulator connected in the inverting buck-boost configuration. The circuit can be designed using the ADIsimPower program available at www.analog.com/ADIsimPower. The L1 coupled inductor is used to develop an unregulated 5 V supply for the circuit using a Zeta configuration. This circuit yields high efficiency for small output currents.

The integral nonlinearity (INL) and differential nonlinearity (DNL) measured at TP2 (bipolar output) are shown in Figure 2 and Figure 3, respectively.

The INL and DNL measured at TP1 (unipolar DAC output) are shown in Figure 4 and Figure 5, respectively.

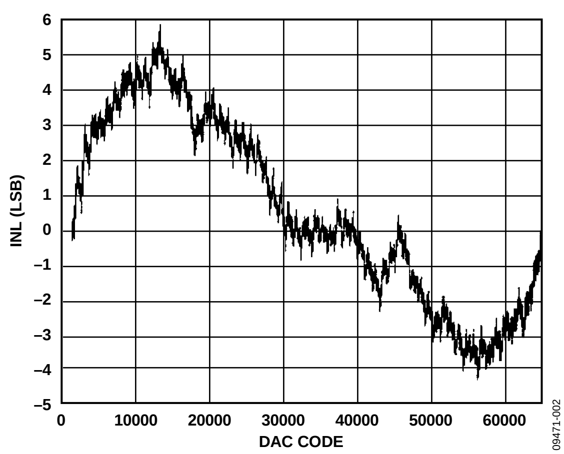

Figure 2. INL Performance of Bipolar Output (TP2)

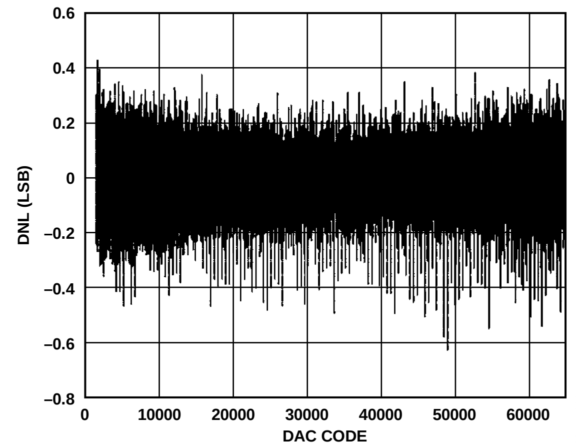

Figure 3. DNL Performance of Bipolar Output (TP2)

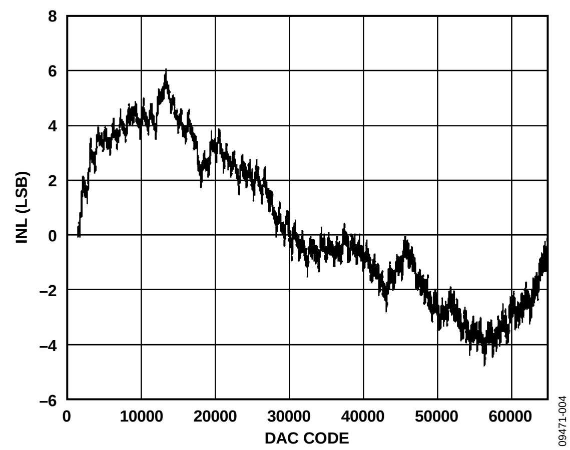

Figure 4. INL Performance of Unipolar DAC Output (TP1)

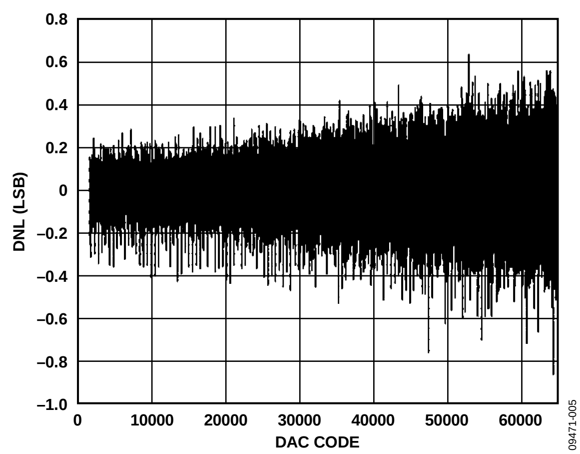

Figure 5. DNL Performance of Unipolar DAC Output (TP1)

COMMON VARIATIONS

The AD5628 and AD5648 are 12-bit and 14-bit versions of the AD5668. All have an on-chip reference with an internal gain of 2. The AD5628-1/AD5648-1/AD5668-1 have a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V; and the AD5628-2/AD5648-2/AD5668-2 and AD5668-3 have a 2.5 V, 5 ppm/°C reference, giving a full-scale output range of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write. The part incorporates a power-on-reset circuit that ensures that the DAC output powers up to 0 V (AD5628-1/AD5648-1/AD5668-1, AD5628-2/AD5648-2/AD5668-2) or midscale (AD5668-3) and remains powered up at this level until a valid write takes place.

The AD8639 is a dual version of the AD8638 and can be used, if desired. The circuit in Figure 1 uses the single AD8638 to minimize crosstalk between the eight channels.

Other 2.5 V references can be used, such as the ADR4525, which has an accuracy of ±0.02% and a temperature coefficient of 2 ppm/°C maximum (B grade).

CIRCUIT EVALUATION AND TEST

Equipment Needed (Equivalents Can Be Substituted)

The following equipment is needed:

- The System Demonstration Platform (EVAL-SDP-CB1Z)
- The CN-0183 circuit evaluation board (EVAL-CN0183-SDZ)
- The CN-0183 evaluation software
- The Tektronix TDS2024, 4-channel oscilloscope
- The HP E3630A 0 V to 6 V/2.55 A; ±20 V/0.5 A triple output dc power supply
- A PC (Windows 32-bit or 64-bit)

Getting Started

Load the evaluation software by placing the CN-0183 evaluation software CD in the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software CD and open the **Readme** file. Follow the instructions contained in the **Readme** file for installing and using the evaluation software. The evaluation software main window is shown in Figure 6.

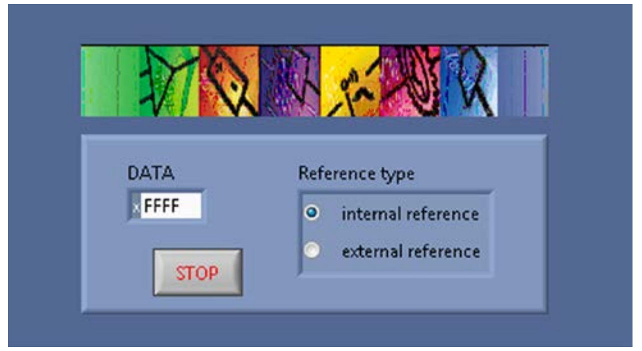

Figure 6. Evaluation Software Main Window

Functional Diagram of Test Setup

A functional diagram of the test setup is shown in Figure 7. This setup allows the DAC output (TP1) and the bipolar output (TP2) to be observed with an oscilloscope.

Linearity measurements require a precision, digital voltmeter (DVM) that can be read by the PC via a USB port.

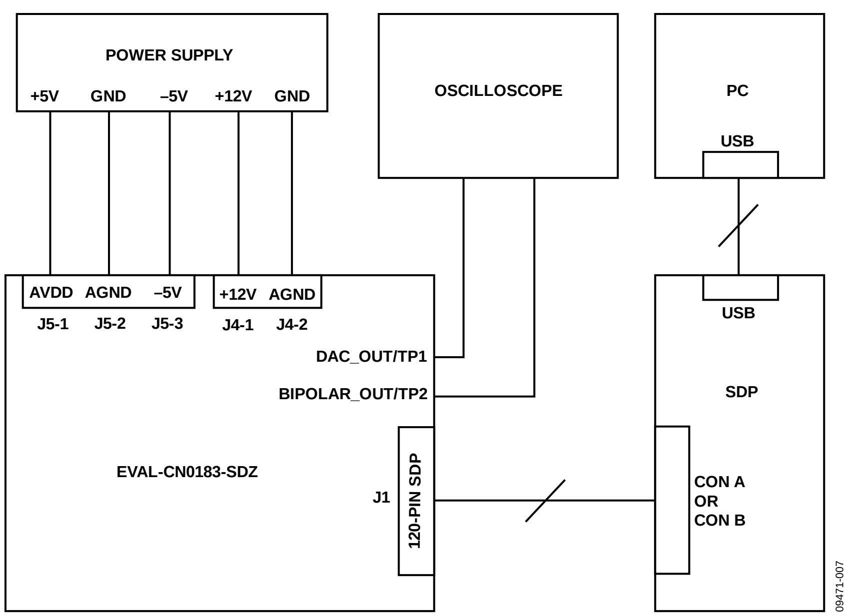

Figure 7. Functional Diagram of Test Setup

Setup

Connect the 120-pin connector on the EVAL-CN0183-SDZ to the **CON A** connector or the **CON B** connector on the EVAL-SDP-CB1Z. Use nylon hardware to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. After successfully setting the dc output supply to +5 V, −5 V, and +12 V, turn the power supply off.

With power to the supply off, connect the −5 V power supply to the −5V pin on J5-3, connect the +5 V power supply to the AVDD pin on J5-1, connect GND to the AGND pins on J5-2 and J4-2, and connect the +12 V power supply to the +12V pin on J4-1. Alternatively, place Link 2 and Link 3 in Position B to power the circuitry using the ADP2300 to supply +5 V and −5 V. Note that AVDD and the −5 V are not needed in this case.

Turn on the power supply and then connect the USB cable from the SDP board to the USB port on the PC. Do not connect the USB cable to the mini-USB connector on the SDP before turning on the dc power supply for the EVAL-CN0183-SDZ.

After setting up the test equipment, connect the probes of the oscilloscope to the TP1 and TP2 test points. The TP3, TP4, and TP5 test points are connected to the reference, the regulated +5 V, and the regulated −5 V, respectively. Check these test points for the correct voltages (use TP6 for the ground).

The software provided on the CD allows users to set the value of $V_{OUT}A$ by loading a code into the DAC and by choosing the source of the reference. If users keep the default setting, they will have to supply the +5 V and −5 V voltages, and the +12 V is not required. The default setting uses the external REF192 reference, giving you a full-scale DAC output range of 2.5 V (TP1), and −2.5 V to +2.5 V on the bipolar output (TP2). Loading 0x0000 sets the DAC output to 0 V and the bipolar output to −2.5 V. Loading 0x8000 sets the DAC output to 1.25 V and the bipolar output to 0 V. Loading 0xFFFF sets the DAC output to 2.5 V and the bipolar output to 2.5 V.

Table 1. Jumper Settings for EVAL-CN0183-SDZ (Default Settings in Bold)

Jumper	Description	Setting	Function
LK1	Short AD5668 reference pin to REF192 output	**Inserted**	**It shorts AD5668 reference pin to REF192 output allowing the use of an external DAC reference.**
		Opened	Only the internal reference of the AD5668 can be used.
LK2	AVDD supply source	**Position A**	**The circuit is powered by an external 5 V supply applied to the AVDD pin on J5-1.**
		Position B	The digital power is supplied by the 5 V voltage supplied by the ADP2300 regulator.
LK5	−5 V voltage source	**Position A**	**The analog circuit is supplied by an external power supply apply to the −5V pin on J5-3.**
		Position B	The digital power is supplied by the −5 V voltage obtained by inverting the output of the ADP2300 regulator.

LEARN MORE

CN-0183 Design Support Package: http://www.analog.com/CN0183-DesignSupport

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

ADIsimPower Design Tool

Data Sheets and Evaluation Boards

CN-0183 Circuit Evaluation Board (EVAL-CN0183-SDZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

AD5668 Data Sheet and Evaluation Board

AD8638 Data Sheet and Evaluation Board

ADP2300 Data Sheet and Evaluation Board

REF192 Data Sheet and Evaluation Board

REVISION HISTORY

6/12—Rev. 0: Initial Version