

*Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit [www.analog.com/CN0213](http://www.analog.com/CN0213).*

| Devices Connected/Referenced |  |
|------------------------------|--|
| AD7685                       | 16-Bit, 250 kSPS PulSAR® ADC in MSOP/QFN                         |
| AD8226                       | Wide Supply Range, Rail-to-Rail Output Instrumentation Amplifier |
| AD8275                       | G = 0.2, Level Translation, 16-Bit ADC Driver                    |
| ADP1720                      | 50 mA, High Voltage, Micropower Linear Regulator                 |
| ADR439                       | Ultralow Noise XFET® Voltage Reference                           |

## Complete High Speed, High CMRR Precision Analog Front End for Process Control

### EVALUATION AND DESIGN SUPPORT

#### Design and Integration Files

[Schematics](#), [Layout Files](#), [Bill of Materials](#)

### CIRCUIT FUNCTION AND BENEFITS

Signal levels in industrial process control systems generally fall into one of the following categories: single-ended current (4 mA-to-20 mA), single-ended, differential voltage (0 V to 5V, 0 V to 10 V, ±5 V, ±10 V), or small signal inputs from sensors

such as thermocouples or load cells. Large common-mode voltage swings are also typical, especially for small signal differential inputs; therefore good common-mode rejection is an important specification in the analog signal processing system.

The analog front-end circuit shown in Figure 1 is optimized for high precision and high common-mode rejection ratio (CMRR) when processing these types of industrial-level signals.

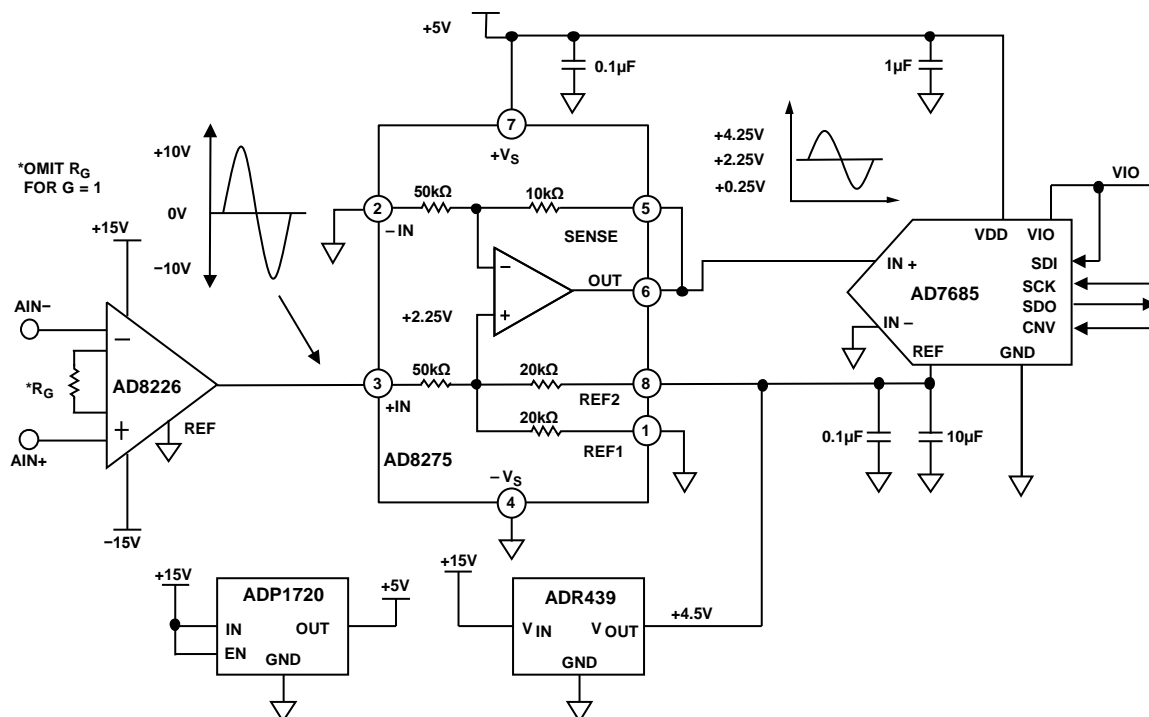


Figure 1. High Performance Analog Front End for Process Control (Simplified Schematic: All Connections and Decoupling Not Shown)

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#### Rev.0

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The circuit level shifts and attenuates the signals so they are compatible with the input range requirements of most modern single-supply SAR ADCs, such as the [AD7685](#) high performance 16-bit 250 kSPS PulSAR® ADC.

With an 18 V p-p input signal, the circuit achieves approximately 105 dB common-mode rejection (CMR) at 100 Hz and 80 dB CMR at 5 kHz.

High precision, high input impedance, and high CMR are provided by the [AD8226](#) instrumentation amplifier. For high precision applications, a high input impedance is required to minimize system gain errors and also to achieve good CMR. The [AD8226](#) gain is resistor-programmable from 1 to 1000.

A resistive level shifter/attenuator stage directly on the input would inevitably degrade CMR performance due to the mismatch between the resistors. The [AD8226](#) provides the excellent CMR required for both small signal and large signal inputs. The [AD8275](#) level shifter/attenuator/driver performs the attenuation and level shifting function in the circuit, without any need for external components.

Traditionally, sigma-delta ADCs have been used in high resolution measurement systems because signal bandwidths are quite low, and the sigma-delta architecture provides excellent noise performance at low update rates. However, there is an increased trend for higher update rates, especially in multichannel systems, to allow faster per-channel update, or for increased channel density. In such cases a high performance SAR ADC is a good alternative. The circuit shown in Figure 1 uses the [AD7685](#) 250 kSPS 16 bit ADC, with the [AD8226](#) high performance in-amp, and the [AD8275](#) attenuator/level shifter amplifier implemented as a complete system solution without the need for any external components.

## CIRCUIT DESCRIPTION

This circuit is comprised of an [AD8226](#) rail-to-rail output in-amp, connected to the positive input of the [AD8275](#)  $G = 0.2$  difference amplifier, whose output is then connected to the input of the [AD7685](#), a 16-bit, 250 kSPS PulSAR ADC in MSOP/QFN. The [AD8226](#) is set for a gain-of-one mode (high voltage/current inputs), and its output is referenced to ground. Single-ended or differential inputs can be used. The output of the [AD8226](#) is a bipolar signal, which drives the [AD8275](#) input. The [AD8275](#) acts to attenuate and level shift the bipolar input, providing for a gain of 0.2. Hence, differential inputs of 20 V p-p

at its inputs will yield a 4 V p-p single-ended range on the output. The [ADR439](#) precision 4.5 V reference is used to provide both the internal common-mode bias voltage for the [AD8275](#) ( $V_{REF}/2 = 2.25V$ ), as well as the external reference voltage for the [AD7685](#) ADC. Under these conditions, the output of the [AD8275](#) swings from +0.25 V to +4.25 V, which is within the range of the [AD7685](#), 0 V to +4.5 V.

The [ADP1720](#) is used to provide the 5 V supply for the [AD8275](#) and the [AD7685](#). The [ADP1720](#) was chosen because it has a high input voltage range (up to 28 V). In this circuit, the [ADP1720](#) is only required to supply approximately 4 mA to the [AD8275](#) and [AD7685](#), so the worst case power dissipation in the regulator with 28 V input is about 90 mW. This allows the complete system to run from the external  $\pm 15$  V supplies.

## System Level Common-Mode Rejection Performance

Initial testing was to verify the performance of the [AD8226](#) common-mode rejection at a system level through to the ADC. Input test tones of 10 Hz, 100 Hz, 500 Hz, 1 kHz, 2 kHz, 3 kHz, 4 kHz, 5 kHz were used, with an 18 V p-p input signal. The test results are summarized in Table 1. In Test 1 the AIN+ and AIN- signals are shorted together and connected to the ac test tone, and the results measured with an FFT. The [AD8226](#) should reject the ac signal because its inputs are connected together. In Test 2 the signal is applied to AIN+, and AIN- is connected to ground. Under these conditions, the FFT measures the level of the tone. The common-mode rejection can then be calculated as the difference in the FFT results between Test 1 and Test 2. Table 1 summarizes the CMR values obtained at different frequencies. It is important to note that the CMR of the [AD8226](#) is specified at 80 dB at 5 kHz, so no loss in CMR performance is realized at the system level.

## System Level AC Performance

The ac accuracy of the system was also tested at a system level with the [AD7685](#) operating at a sampling rate of 250 kSPS. Figure 2 shows an FFT test result for a 5 V p-p input at 10 kHz. The results shown in the plot are given below:

- SNR = 87.13 dBFS
- SINAD = 85.95 dBFS
- SFDR = 81.82 dBc
- THD = -78.02 dBc

Table 1. CMR Performance of Circuit for 18 V p-p Input

| Frequency (kHz) | FFT Signal Level (dBFS), 18 V p-p Input |                                     | CMR (dB) |
|-----------------|---|-------------------------------------|----------|
|                 | Test 1:<br>AIN+ = AIN-                  | Test 2:<br>Input = AIN+, AIN- = GND |          |
| 0.1             | -104.64                                 | -2.86                               | 101.78   |
| 0.5             | -100.00                                 | -3.28                               | 96.72    |
| 1               | -94.67                                  | -2.85                               | 91.82    |
| 2               | -88.58                                  | -2.88                               | 85.70    |
| 3               | -84.93                                  | -2.93                               | 82.00    |
| 4               | -82.07                                  | -3.01                               | 79.06    |
| 5               | -79.43                                  | -3.10                               | 76.33    |

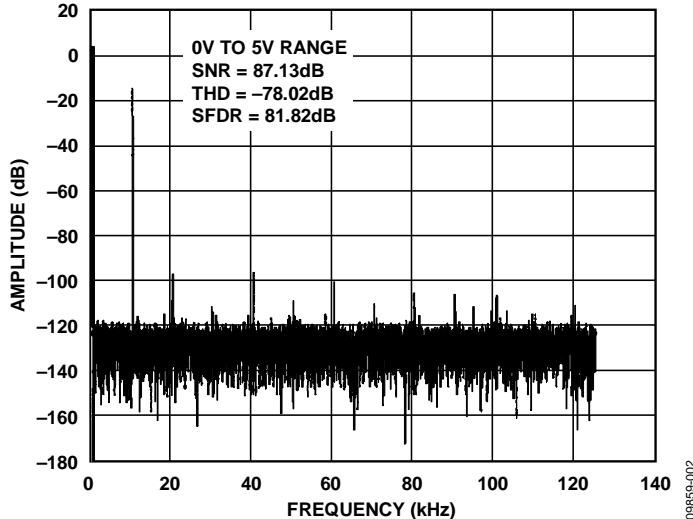


Figure 2. FFT Results for 10 kHz Input Signal 14 dB Below Full-Scale, 250 kSPS Sampling Rate

The performance of this or any high speed circuit is highly dependent on proper PCB layout. This includes, but is not limited to, power supply bypassing, controlled impedance lines (where required), component placement, signal routing, and power and ground planes. (See [MT-031 Tutorial](#), [MT-101 Tutorial](#), and article, [A Practical Guide to High-Speed Printed-Circuit-Board Layout](#), for more detailed information regarding PCB layout.)

A complete design support package for this circuit note can be found at <http://www.analog.com/CN0213-DesignSupport>.

## COMMON VARIATIONS

This circuit is proven to work well with good stability and accuracy with component values shown. Other ADI analog-to-digital converters can be used in place of the [AD7685](#) to achieve even higher speed/resolution or higher performance. The [AD7688](#) provides a true differential input to achieve even better CMR. The [AD7982](#) 18-bit ADC provides higher resolution at speeds up to 1 MSPS and is also fully differential. The [AD8475](#) funnel amplifier can also accept high voltage bipolar inputs and provide attenuation and level shifting with differential outputs, making it ideal for industrial applications using ADCs with differential inputs (See [Circuit Note CN-0180](#)).

## CIRCUIT EVALUATION AND TEST

The circuit was tested using the System Demonstration Platform (SDP). The SDP platform includes the necessary ADC drivers and also the USB connectivity to the PC. Sampled data from the ADC is sent to the PC via USB using the SDP board. The FFT plots were generated using the standard ADC LabVIEW evaluation software tools available from ADI. A functional block diagram of the test setup is shown in Figure 3 and a photograph of the boards in Figure 4.

### Equipment Used to Collect Test Data

- PC with a USB port and Windows® XP or Windows Vista® (32-bit), or Windows® 7 (32-bit)
- EVAL-A-INPUT-1AZ circuit evaluation board
- EVAL-SDP-CB1Z, SDP-A evaluation board
- Evaluation software
- Power supply: +5 V @ 200 mA.
- Power supply: ±15 V, Agilent E3630A or equivalent
- Signal generator: Agilent 33120A or equivalent

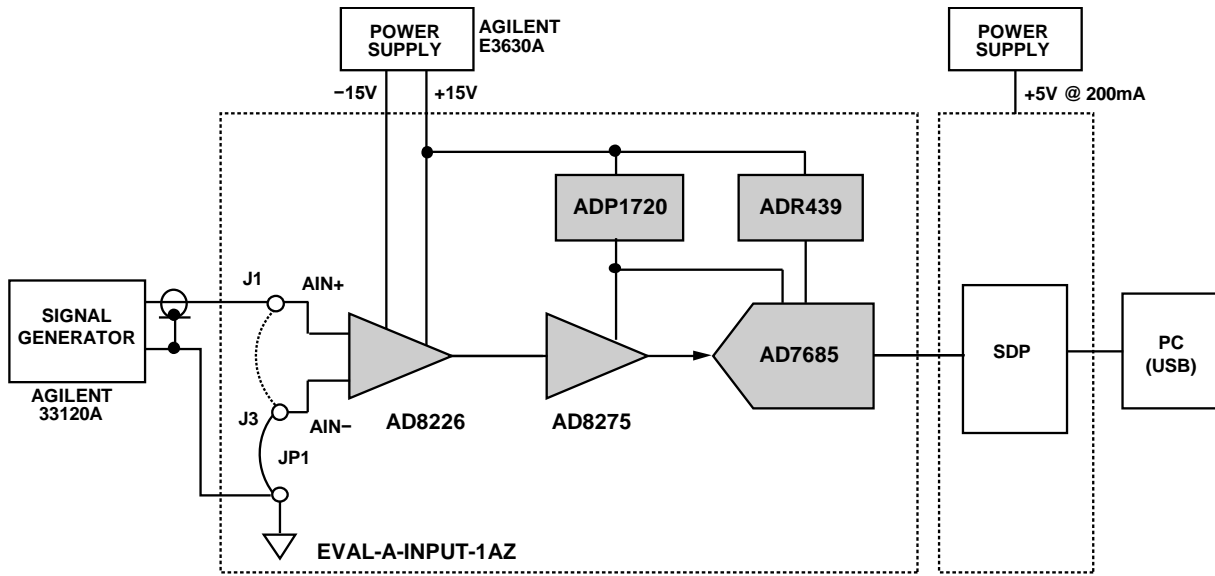


Figure 3. Functional Block Diagram of Test Setup

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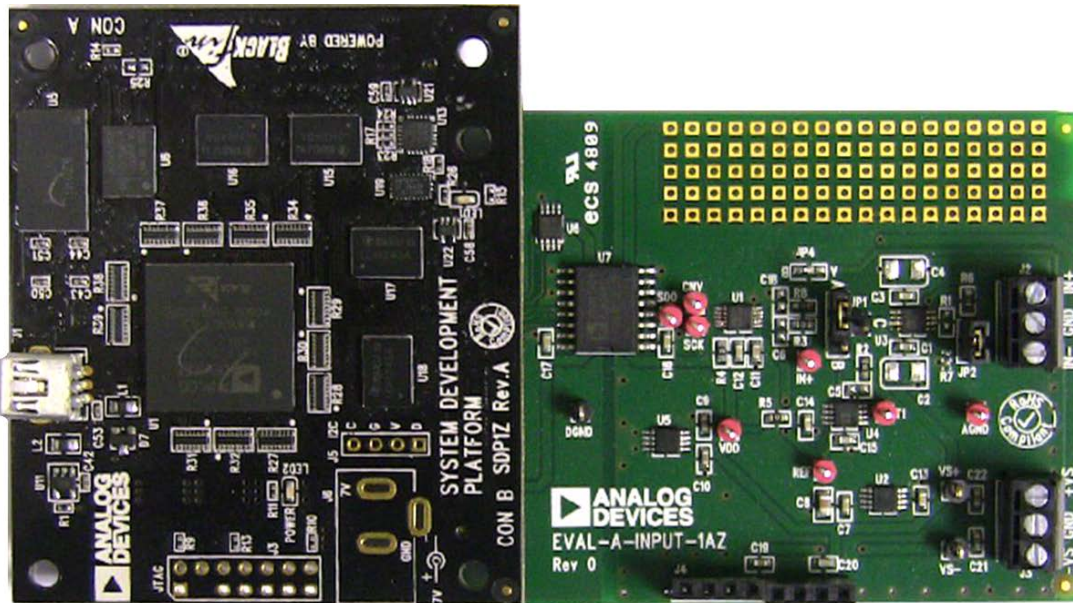


Figure 4. Photo of EVAL-A-INPUT-1AZ Evaluation Board Connected to SDP Board

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**Setup and Test**

Evaluation software was loaded in the CD drive of the PC.

The 120-pin connector on the EVAL-A-INPUT-1AZ circuit board was connected to the connector marked "CON B" on the EVAL-SDP-CB1Z evaluation (SDP) board. Nylon hardware was used to firmly secure the two boards, using the holes provided at the ends of the 120-pin connectors. The signal source was connected to the EVAL-A-INPUT-1AZ board J1 input (AIN+) terminal. When running normal FFT tests, the JP1 jumper was connected between the J3 terminal (IN-) and ground. When running CMR tests, the jumper was connected between J1 (AIN+) and J3 (AIN-).

With power to the supply off, a +5 V power supply was connected to the SDP board. The USB cable was used to connect the SDP board to the USB port on the PC.

The ±15 V supplies were then connected to EVAL-A-INPUT-1AZ circuit board. The evaluation software was launched, and the USB cable was connected from the PC to the USB mini-connector on the SDP board.

Once USB communications are established, the SDP board was used to send, receive, and capture serial data from the EVAL-A-INPUT-1AZ board.

**LEARN MORE**

CN-0213 Design Support Package:

<http://www.analog.com/CN0213-DesignSupport>

Ardizzoni, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, *Analog Dialogue* 39-09, September 2005.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

**Data Sheets and Evaluation Boards**

System Demonstration Platform (EVAL-SDP-CB1Z)

[AD7685 Data Sheet](#)

[AD7685 Evaluation Board](#)

[AD8226 Data Sheet](#)

[AD8275 Data Sheet](#)

**REVISION HISTORY**

7/11—Revision 0: Initial Version

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CN09859-0-7/11(0)



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