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Optimum MOSFET Selection for Synchronous Rectification

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Updated all 4-quadrant-graphs. And performed some small formatting changes.

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1 Introduction

Due to continuous increase of the packaging density of power converters and the more and more restricted energy saving guidelines, the efficiency of power stages has to be successively improved. As the high diode forward losses of the secondary side rectification of an isolated converter are the main losses, this efficiency level is only possible with synchronous rectification (often shortened to 'Sync. Rec.' or even 'SR'). Replacing the diodes by MOSFETs lead to new challenges – optimizing system efficiency and controlling voltage overshoots. This application note helps to choose the best MOSFET by using optimization charts for the Infineon OptiMOS™ technology for 30 V, 40 V, 60 V, 75 V, 80 V, 100 V, 120 V and 150 V devices.

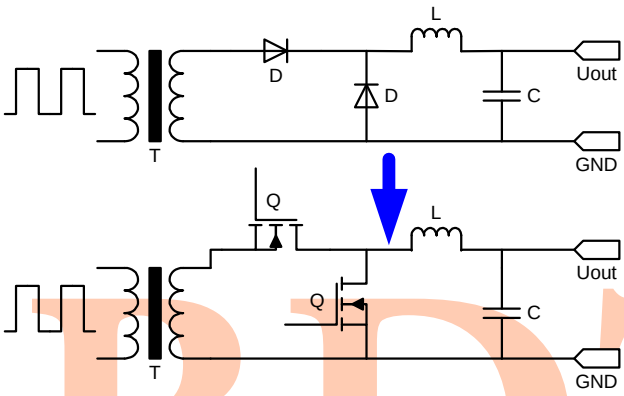

Figure 1. Diode vs. synchronous rectification

2 Basics of Synchronous Rectification

In order to choose the optimum MOSFET in the synchronous rectification, the power loss mechanism needs to be well understood. First of all, the losses have to be distinguished between load dependant conduction losses and quasi constant switching losses. Conduction losses are given by the $R_{DS(on)}$ of the MOSFET and the forward voltage of the internal body diode, V_{SD}. As the output current is getting higher, the conduction losses ($R_{DS(on)}$ losses) are increasing. For assuring an interlock between the two SR MOSFETs and therefore avoiding a current shoot through, a certain dead time has to be guaranteed. Therefore the respective MOSFET has to be switched off before the primary side is turned on. As exactly this MOSFET is conducting the whole freewheeling current, this current has to commutate from the MOSFET channel to the internal body diode, where the additional body diode losses are generated. Due to the very short on-time of the body diode of about 50ns to 100ns, these losses can be neglected if the output voltage is significantly larger than the forward voltage of the body diode.

Depending on the switching frequency (f_{SW}) and the output load (I_{OUT}) of the power converter, switching losses have a big impact on the total losses of a MOSFET. For turning it on, the gate needs to be charged to the

gate-charge, Q_g., so we need to make sure that the gate voltage (V_g) is set high enough for it to happen. For turning the MOSFET off, the gate will be discharged to source, which means a dissipation of the Q_g in the gate-resistance and in the driver. These gate drive losses are higher for low ohmic MOSFETs of a given technology than for higher ohmic MOSFETs, as a larger die size leads to a larger Q_g.

Another important portion of the total switching losses is related to the output capacitance C_{oss} and the reverse recovery charge Q_{rr} of the MOSFET. Considering the turn-off moment, the Q_{rr} has to be removed and the output capacitance has to be charged up to the secondary side transformer voltage (V_T). This process results in a reverse current peak, which couples to the inductances in the commutation loop. Hence this energy is transferred to the output-capacitance of the MOSFET and a voltage spike occurs carrying the energy stored beforehand. This energy is triggering a LC oscillation circuit, defined by the inductances of the PCB and the MOSFET output capacitance C_{oss}. The oscillation gets damped by the parasitic series resistance of the circuit. As this inductive turn-off energy is directly dependant on the MOSFET C_{oss} – respectively the output charge Q_{oss} when charged up to the secondary side transformer voltage - the total C_{oss} defines the capacitive turn-off losses. Similarly to what happens with the gate-charge, Q_{oss} increases for low ohmic devices. Therefore, it is always possible to find a balance between conduction and switching losses that achieves maximum efficiency.

As a first approximation, Qrr can be neglected for OptiMOS™ products, as it just has a minor contribution to the total power losses. In this case the Qrr is considered as only the MOSFET body diode reverse recovery charge, whereas the Qrr on datasheets is measured confirming JEDEC standards and therefore contains not only the body diode Qrr but also some part of the output charge of the MOSFET. Further circumstances lead to a decrease of the real Qrr value in the application, compared to the Qrr value on datasheets. Datasheet values are measured by applying the maximum allowable MOSFET drain current, the body diode is conductive a very long time up to 500µs and the di/dt is fixed to a value of 100A/µs. Going to the real application, currents of about a third of the maximum drain current or less are most typically seen, the body diode conduction time is in the range of 20ns to 100ns and the di/dt can reach values of 800A/µs.

3 Optimization of the Synchronous Rectification MOSFET

For optimizing the SR MOSFET regarding efficiency, a well balanced ratio between switching losses and conduction losses has to be found. Considering light load condition, the $R_{DS(on)}$ conduction losses play just a minor role. In this case the switching losses, which are more or less constant over the whole load range, are dominant. In case of high output current the conduction losses are the biggest portion and therefore contribute most to the total power losses, see figure 2.

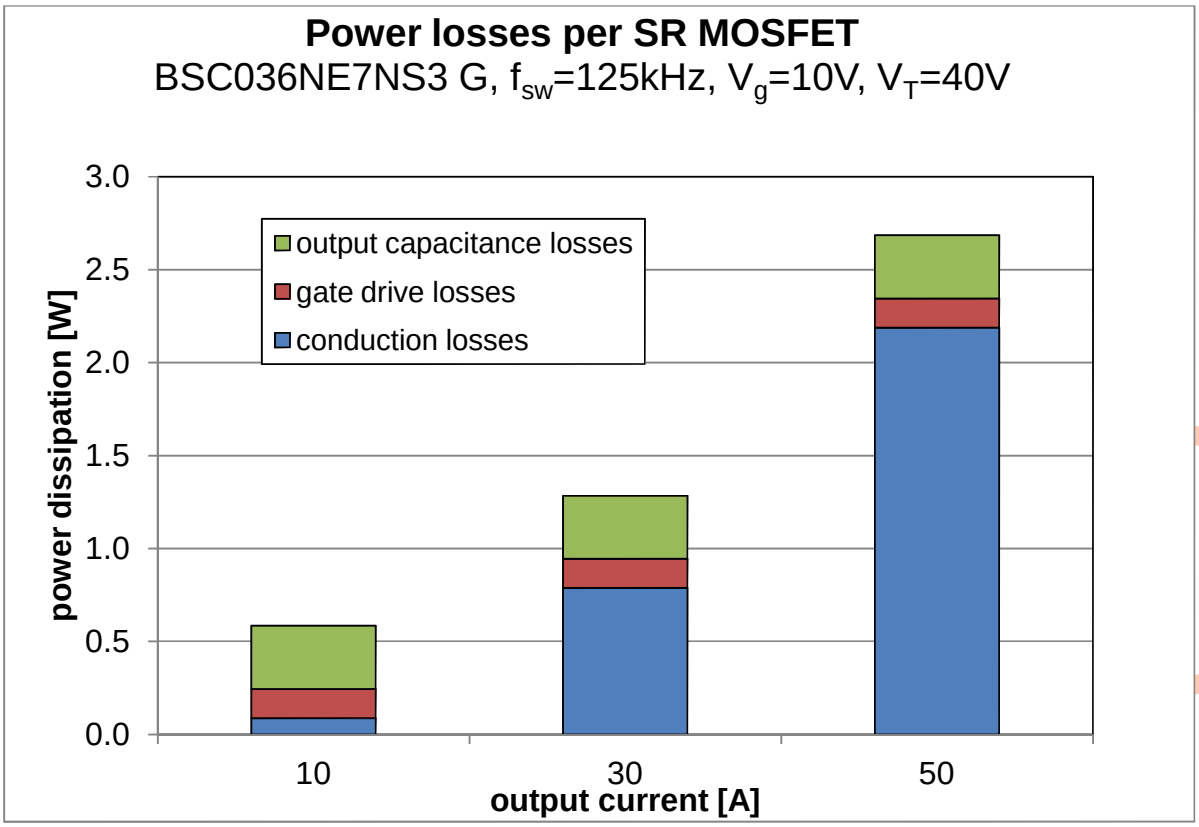

Figure 2. Power Loss Breakdown vs. Output Current

For choosing the best fitting MOSFET, special attention has to be given to the $R_{DS(on)}$class. As an example, we will use the 60V OptiMOS family under certain conditions, as illustrated in figure 3. Going beyond the optimum point will increase total power losses with the $R_{DS(on)}$ linearly. But, in our example, lowering the $R_{DS(on)}$ below 0.5 mΩ will lead to dramatically increased losses because of rapidly increasing output capacitance. Furthermore, in figure 3 can be seen that the range of minimum power losses is quite wide. In this example, total losses stay roughly the same between 0.75 mΩ and 2.8 mΩ, which means that both the BSC016N06NS and BSC028N06NS would be suitable. And, actually, since losses are still below 1W over a broader range (0.55 mΩ to 3.9 mΩ), selecting the BSC039N06NS is also acceptable. But the BSC039N06NS performs better in applications with lower current and/or higher switching frequency.

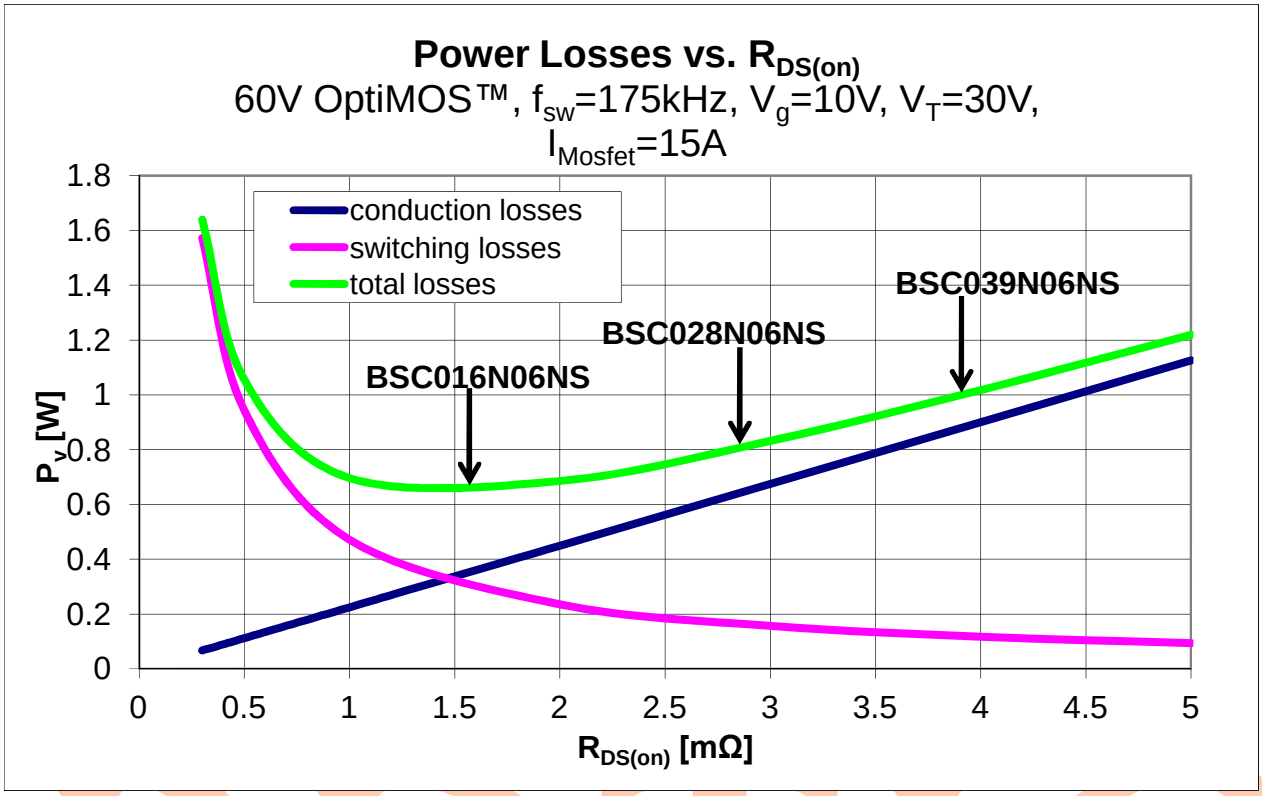

Figure 3. Power Losses vs. $R_{DS(on)}$

In any case, one must never forget that graphs such as figure 3 are plotted under specific conditions. Indeed, as can be seen on figure 4, the situation changes greatly when varying the switching frequency (see 4a and 4b) or the current flowing through each MOSFET (see 4c and 4d),

If we take the example of figure 4a where I_{Mosfet} is decreased to 5A (f_{sw} stays at 175kHz), switching losses now represent a bigger share of the overall losses, so it is advantageous to opt for the BSC039N06NS. On the other hand, when the switching frequency is reduced to 100kHz (I_{Mosfet} stays at 15A) as in figure 4c, a part that exhibits lower conduction losses such as the BSC016N06NS performs much better.

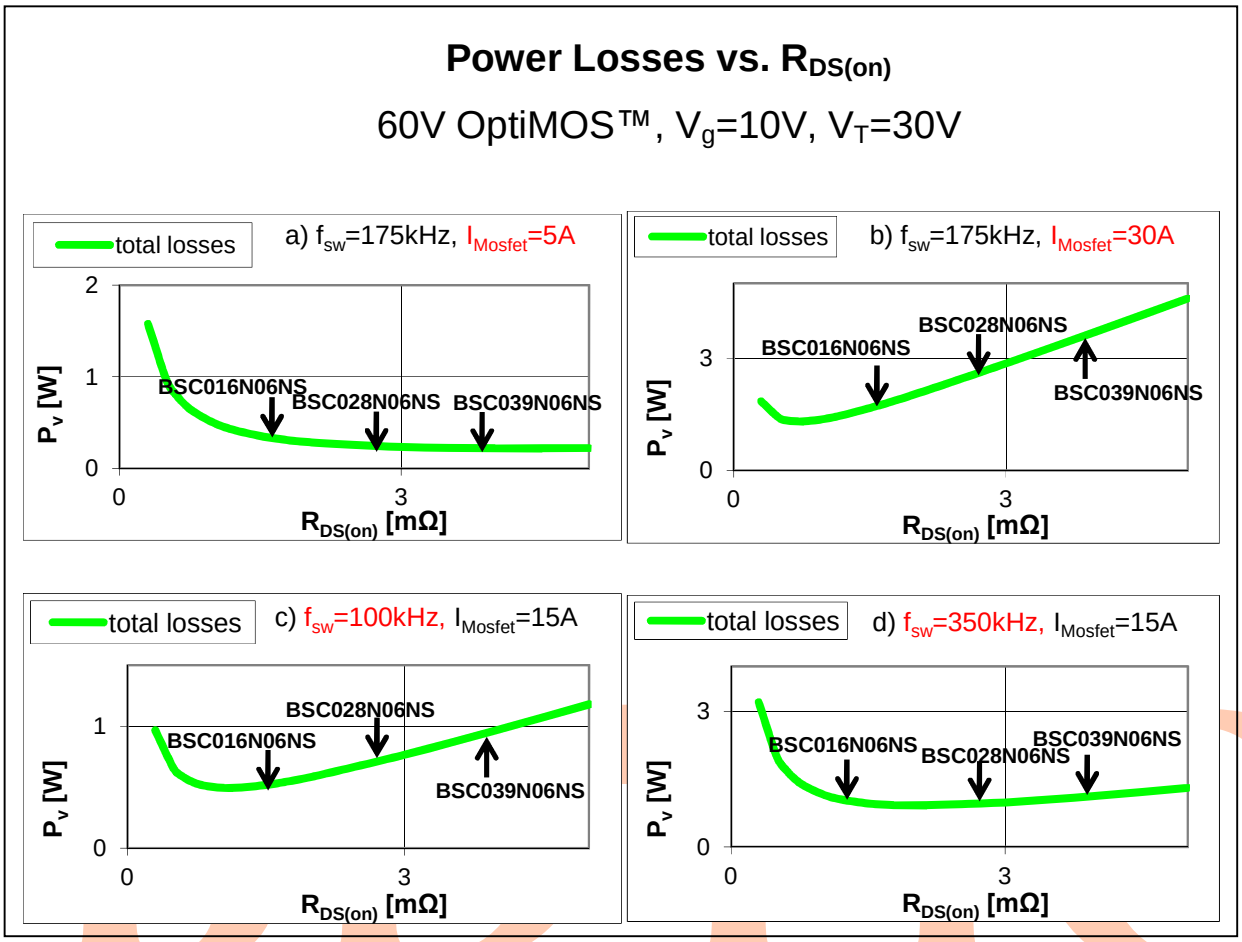

Figure 4. Power Losses vs. $R_{DS(on)}$ at different f_{sw} and I_{Mosfet}

A further important issue for optimizing SR is the correct choice of the MOSFET package. Indeed, an efficiency boost can be achieved simply by replacing the TO-220 package with a SuperSO8. The reason for this is the reduced package contribution to the total $R_{DS(on)}$ in case of the SuperSO8 package. Reducing the $R_{DS(on)}$ while keeping the output capacitance the same, leads to a reduced FOM_{Qoss} , which is a performance indicator of a given MOSFET technology (FOM_{Qoss}= $R_{DS(on)}$ * Q_{oss}). Reducing the FOM_{Qoss} will then reduce switching losses and therefore increase the efficiency.

4 At which load current should the MOSFET be optimized?

To achieve a balanced efficiency over the whole load range, a reasonable choice of the MOSFET current in the four quadrant SR device optimization chart has to be done. Going for a full load optimization will give good efficiency results at high output currents. But this approach will dramatically decrease efficiency at low loads

and increase the number of parallel MOSFETs to an unacceptable value. Therefore an optimum has to be found, in order to achieve a relative constant efficiency value over the whole output current range.

To illustrate this problem, efficiency curves with different optimization approaches can be seen in figure 5. These efficiency charts show the calculated efficiency of a synchronous rectification stage with an output voltage (V_{OUT}) of 12V, a transformer voltage of 24 V, a gate driving voltage of 10 V and a switching frequency of 200 kHz. Taking the BSC010N04LS in the 40 V optimization chart and executing the design process for 20 A MOSFET current will give a single MOSFET as an optimum. Shown in figure 5, this gives high efficiency at low currents but lower efficiency at high currents. Going for a 40 A optimization will give an optimum number of MOSFETs of 2. In this case, the efficiency at low currents decreases, but reaches maximum at higher load.

Typically a balanced efficiency can be achieved by optimizing the MOSFET for 20 % to 30 % of the maximum output power. For systems with focus on light load efficiency, currents as low as 10 % to 20% of the maximum current can be used, while for high load designs, optimization of up to 60 % may be suitable. An optimization for 100 % output load should be avoided, as low load efficiency is suffering and the number of parallel MOSFETs is highly increased.

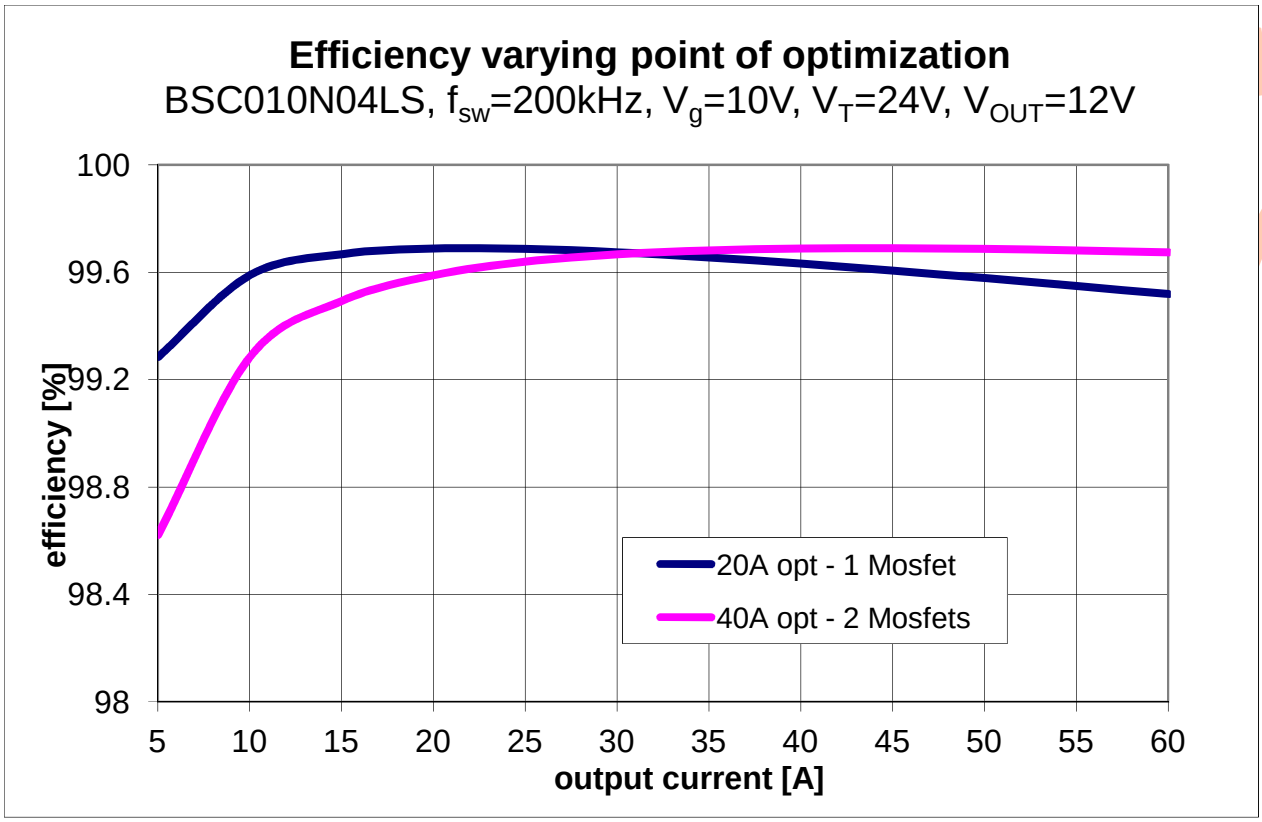

Figure 5. Efficiency varying point of optimization

5 MOSFET Selection by Using a Four Quadrant SR Device Optimization Chart

For easier selection of the optimum MOSFET in the SR application, we shall now introduce a four quadrant SR device optimization chart. With this chart it is possible to find the best fitting part by using three application parameters: secondary side transformer voltage, switching frequency and RMS MOSFET current. For an easier understanding a worked example is done in figure 6.

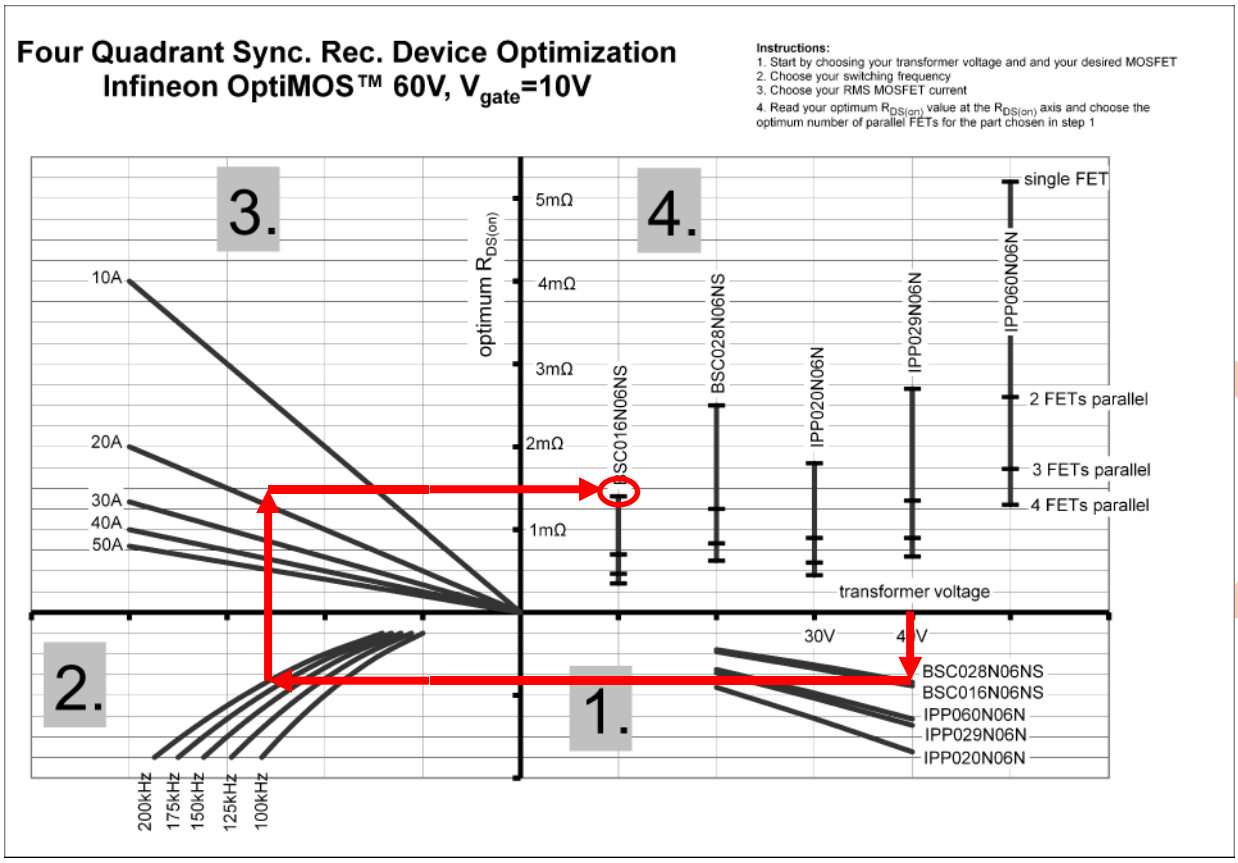

Figure 6. Four Quadrant SR Device Optimization Chart

Starting point for the optimization chart is the secondary side transformer voltage. By drawing a vertical line, at the voltage used, a specific MOSFET can be chosen at the crossing of the two lines. With a horizontal and a further vertical line, switching frequency and MOSFET current can be selected. As previously discussed, a good starting point for the current level is 20 % - 30 % of full load. Now the optimum $R_{DS(on)}$ can be read at the positive y-axis. By looking into field number 4, the optimum number of parallel MOSFETs can be seen. It is important that in this fourth field, the MOSFET which was chosen previously in the first field, is taken as the result. If this procedure is repeated with the same parameters (transformer voltage, switching frequency and

RMS current) but with another MOSFET, the result which gives the lowest optimum $R_{DS(on)}$, produces minimum power losses and is therefore more efficient.

This MOSFET selection routine is calculated for applications with optimum switching behavior. If any second order effects like dynamic turn-on or avalanche is occurring, this chart may be inaccurate. Furthermore best results are achieved for hard switched converter topologies. Any resonant soft switching topology might lead to a mismatch as some part of the switching energy can possibly be recovered. In this case the optimum $R_{DS(on)}$ class will be lower than in the calculation. Note, that a quasi resonant topology on the primary side (e.g. Phase Shift ZVS Full Bridge) can also exhibit hard switching behavior on the secondary side synchronous rectifiers and can therefore be optimized with these design charts.

All results coming out from this optimization chart are based on ideal MOSFET behavior. According to experience, results can differ in real applications compared to ideal calculations. Therefore these results should be considered as an indication for best possible device selection and as a prevention for under/oversizing of the MOSFETs. If the result of the chart is between 2 different numbers of parallel MOSFETs, the lower number will be low-load optimized, while the higher number will be better at high powers. Furthermore, any snubber networks paralleled with the synchronous rectifiers can affect the devices selection and therefore have to be considered.

An optimization over the whole load range cannot be done in one calculation. A specific load point (current level) has to be taken, at which the MOSFET is calculated. For expanding the optimization range, multiple tests on the four quadrant diagram for different load currents need to be carried out and the results have to be referred to the application requirements.