CoolMOS™ 900V

New 900V class for superjunction devices

A new horizon for SMPS and renewable energy applications

Power Management & Supply

Never stop thinking

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CoolMOS™ 900V

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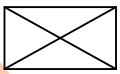

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1 Introduction

Infineon introduces a new 900V voltage class of energy-saving CoolMOS™ power MOSFETs for high efficiency switch-mode power supply and renewable energy applications.

CoolMOS™ 900V offers extremely low static and dynamic losses, which is the signature of super junction MOSFET technology where the so-called “silicon limit” is overcome. The square-law dependency between on-resistance and blocking voltage in conventional MOSFETs is amended by new CoolMOS™ 900V, resulting in an industry-best on-state resistance per package type being four times or even lower if compared to conventional 900V MOSFETs: 0.12 Ohm in TO247, 0.34 Ohm in TO220, and 1.2 Ohm in DPAK packages. A figure-of-merit (FOM) on-resistance times gate charge (R_{DSon}*Q_G) as low as 34 Ω*nC is reached, which translates into extremely low conduction, driving and switching losses.

Samples are available now and the complete product spectrum will be filled up during 2008.

Target applications for CoolMOS™ 900V are ATX power supplies, solar converters, quasiresonant flyback designs for LCD TV, active frontend 3-phase-systems and other designs, were high blocking voltage, low conduction and switching losses combined with low gate charge are necessary.

Table 1 gives a quick overview of available CoolMOS™ series today.

Table 1 CoolMOS™ Series at a Glance

	Market Entry	Voltage Class [V]	Special Characteristic	$V_{gs,th}$ [V]	G_{fs} [S]	Internal R_g [Ω]
CoolMOS™ S5	1998	600	Low $R_{DS(on)}$, Switching speed close to standard MOSFETs	4.5	Low	High
CoolMOS™ C3	2001	500/600/ 650/800	Fast switching speed symmetrical rise/fall time at V_{GS}=10 V	3	High	Low
CoolMOS™ CFD	2004	600	Fast body diode, Q_{rr} 1/10th of C3 series	4	High	Low
CoolMOS™ CP	2005	500/600	Ultra-low *R*DS(on), ultra-low *Q*g, very fast switching speed	3	High	Low
CoolMOS™ C3	***2008***	***900***	***low RDS(on), low Qg, fast switching speed***	***3***	***High***	***Low***

1.1 The Superjunction Principle

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs and designed according to the superjunction (SJ) principle [1], which in turn is based on the RESURF [2] ideas being successfully used for decades in lateral power MOSFETs. Conventional power MOSFETs suffer from the limitation of the so-called “silicon limit” [3], which means that doubling the voltage blocking capability typically leads to an increase in the on-state resistance by a factor of five. The “silicon limit” is shown in Figure 1 where the area specific on-state resistance of state-of-the-art standard MOSFETs as well are indicated. SJ technology may lower the on-state resistance of a power MOSFET virtually towards zero. The basic idea is to allow the current to flow from top to bottom of the MOSFET in very high doped vertically arranged regions. In other words, a lot more charge is available for current conduction compared to what is the case in a standard MOSFET structure. In the blocking state of the SJ MOSFET, the charge is counterbalanced by exactly the same amount of charge of the opposite type. The two charges are separated locally in the device by a very refined technology, and the resulting structure shows a laterally stacked fine-pitched pattern of alternating arranged p- and n-areas, see Figure 2. The finer the pitch can be made, the lower the on-state resistance of the device will be.

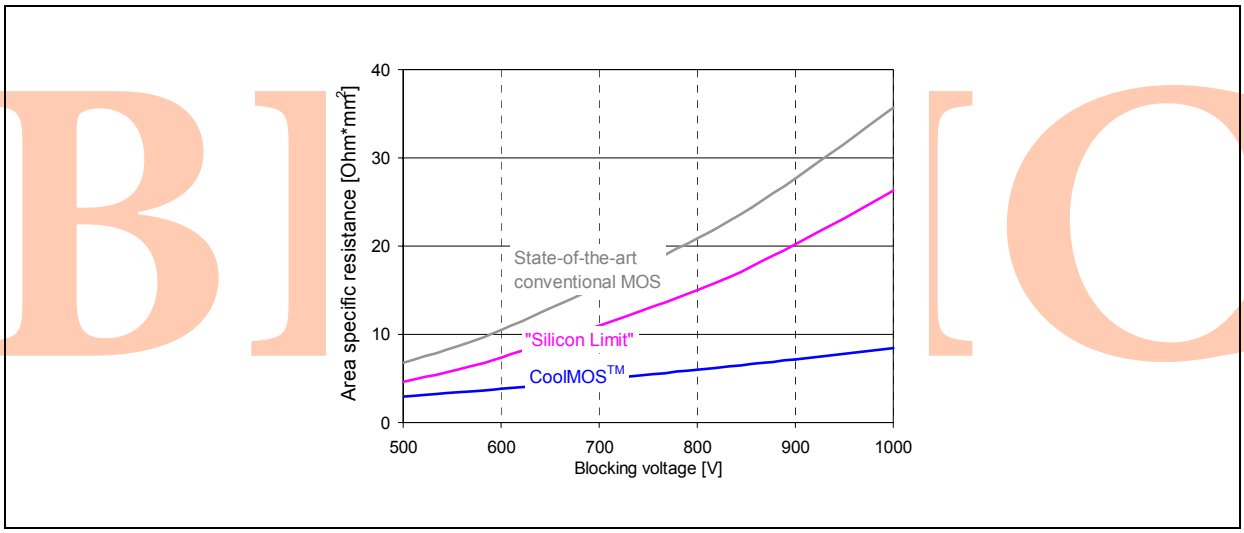

Figure 1 Area-specific on-resistance versus breakdown voltage comparison of standard MOSFET and CoolMOS™ Technology

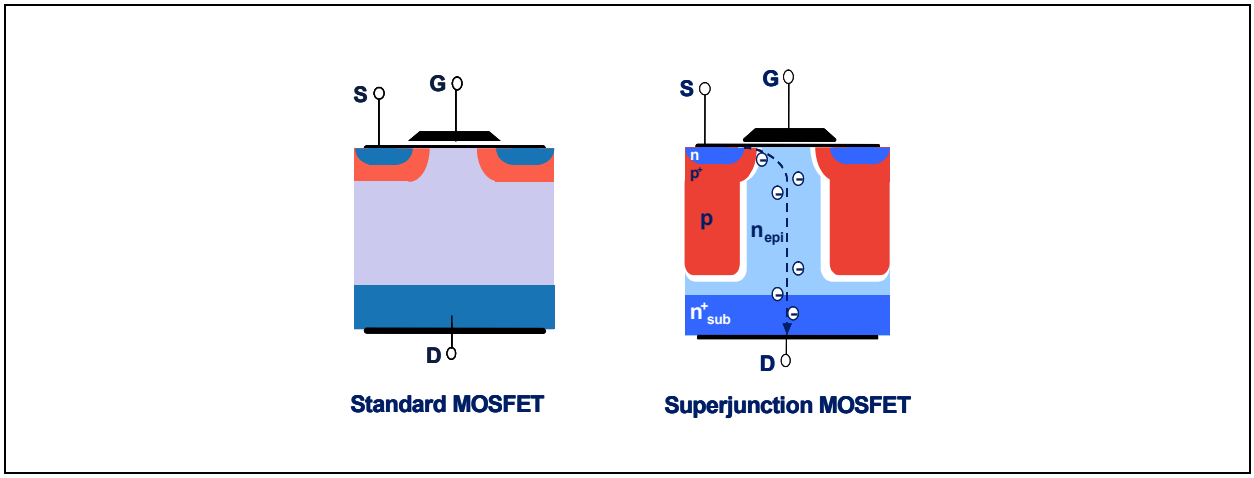

Figure 2 Schematic Cross-Section of a Standard Power MOSFET versus a Superjunction MOSFET

Another signature of SJ technology is the extremely fast switching speed. The turn off behavior of a SJ MOSFET is not characterized by the relatively slow voltage driven vertical expansion of the space charge layer but by a sudden nearly intrinsic depletion of the laterally stacked p-n structure. This unique behavior makes the device very fast. The neutralization of these depletion layers is done via the MOS controlled turn-on of the load current for the n-areas and via a voltage driven drift current for the p-areas. SJ devices reach therefore theoretical rise and fall times in the range of few nanoseconds.

Figure 3 shows a comparison of $R_{DS(on),max}$ between today's most advanced available MOSFETs.

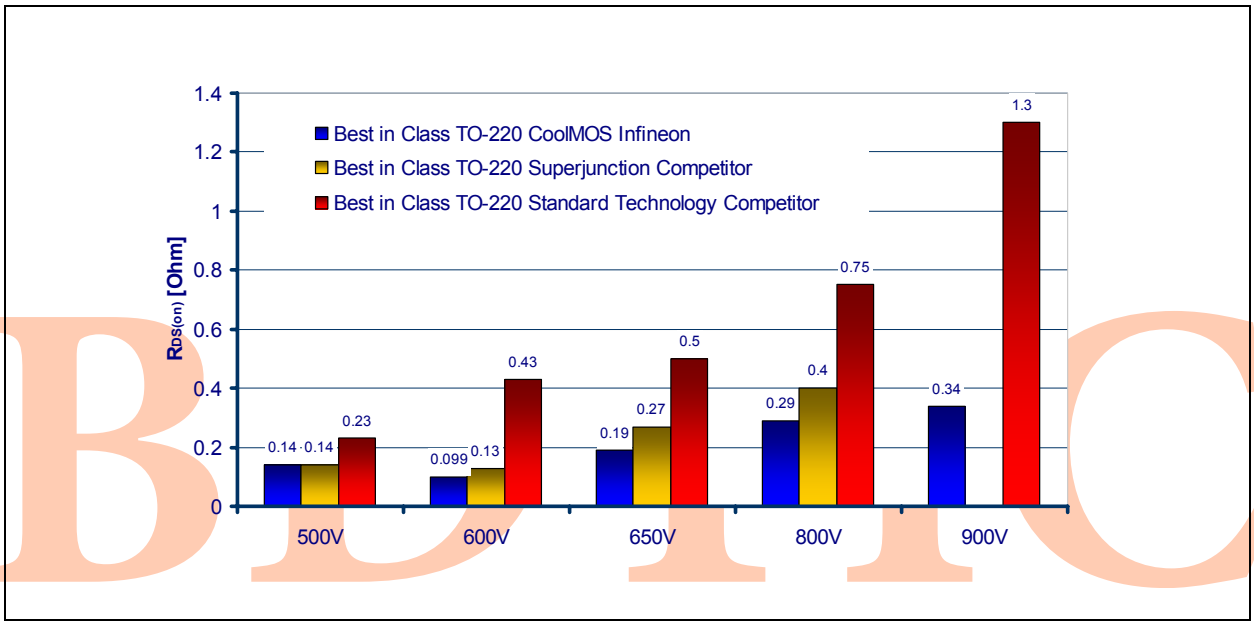

Figure 3 Comparison of $R_{DS(on),max}$ for most advanced MOSFETs in TO220 package available in the market.

2 Device characteristics

CoolMOS™ 900V is the next step towards THE IDEAL HIGH VOLTAGE SWITCH with key features:

- ✓ Very low conduction and switching losses
- ✓ Lowest on-state-resistance per package @ 900 V blocking capability
- ✓ Ultra-low gate charge and lowest figure-of-merit $R_{DS(on)}$ x Q_g

… which gives the application benefits:

- ✓ Extremely reduced heat generation
- ✓ Reduced system size and weight
- ✓ Very low gate drive power facilitating the use of low cost ICs and gate drivers
- ✓ Reduced overall system cost

The most interesting circuit design aspect is that the more than square-law dependency of the area-specific on-resistance ($R_{DS(on)}$ x A) on the breakdown voltage in the case of standard MOSFETs has been amended and a close to linear proportionality has been achieved:

$$R_{DS(on)} \cdot A \propto (V_{Br})^n \qquad n = \begin{cases} 2{,}4...2{,}6 & \text{Standard MOS} \\ 1{,}3 & \text{Cool MOS}^{TM} \end{cases}$$

It follows from this that the on-state losses P_{stat} present in the switch when transferring a particular power are:

$$P_{stat} \propto I_{sw,eff}^{\ 2} \cdot R_{DS(on)} \propto P_{out}^{\ 2} \cdot V_{Br}^{\ n-2}$$

Therefore, whereas the losses increase with the operating voltage when using a standard MOSFET(proportional to $V^{0,4...0,6}$), the losses are reduced using CoolMOS™ transistors proportionally to $V^{-0,7}$.

CoolMOS™ 900V series has the world's lowest area-specific $R_{DS(on)}$ for 900V MOSFETs as shown Figure 4, which results in lowest $R_{DS(on)}$ per package type. 120mΩ in TO247 and 340mΩ in TO220 result in low conduction losses and high current handling capability. Continuous drain currents up to 36A and pulse currents up to 96A are possible (CoolMOS™ 900V 120mΩ). A comparison of available $R_{DS(on)}$-values in DPak, TO220 and TO247 are given in Figure 4.

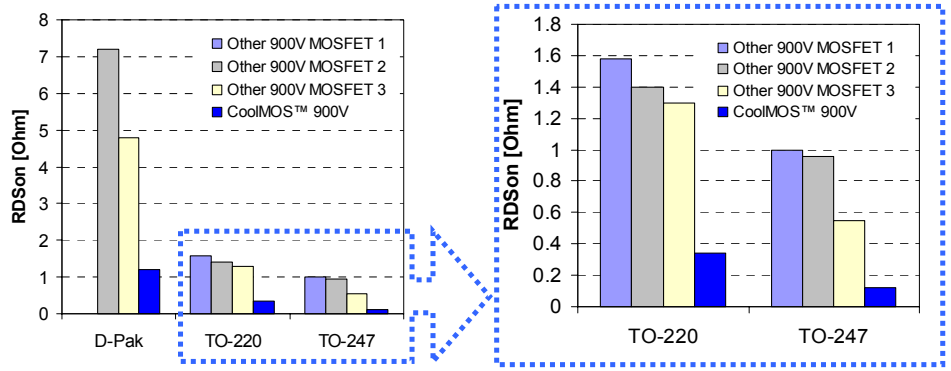

Figure 4 Comparison of $R_{DS(on),max}$ for best-in-class 900V devices (Right: Zoom-in TO220/TO247)

The CoolMOS™ 900V cuts down the achievable $R_{DS(on)}$ in both packages by nearly a factor of four. By introducing our new CoolMOS™ 900V technology we establish also a reduction of the total gate charge. The new technology reduces the total gate charge Q_g for similar $R_{DS(on)}$ types by 25% (Figure 5) and offers the lowest FOM ($R_{DS(on)} \times Q_g$) in this voltage class. The FOM on the one hand a measure of the conduction losses attributed to the switch, on the other hand it correlates with the Q_g a parameter being related to the energy the driver circuit has to offer to turn the switch on and off. A very low FOM stands therefore for low conduction losses, easy driving and low switching losses.

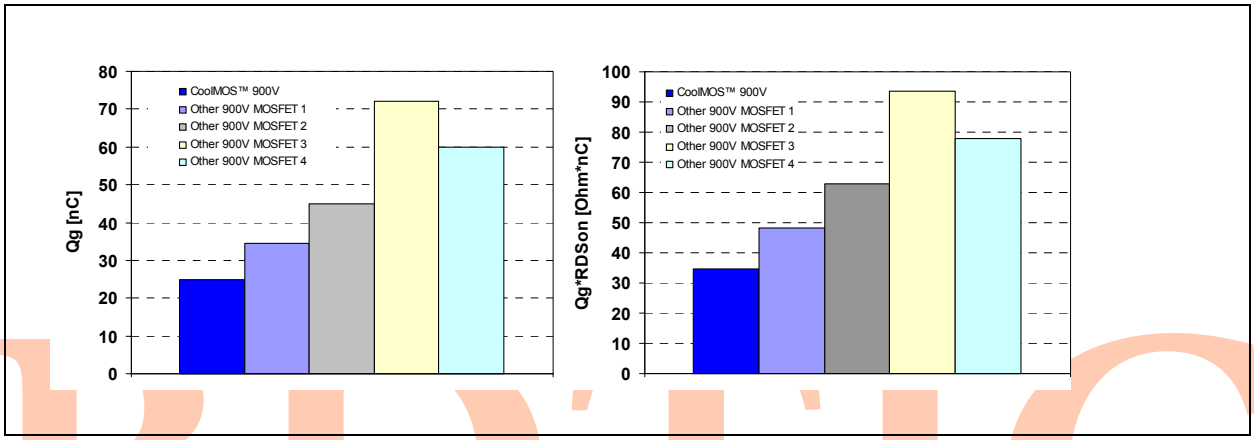

Figure 5 Gate Charge Q_G and Figute-of-merit ($R_{DS(on)}$ x Q_G) values for 900V devices with nearly same $R_{DS(on)}$ of 1.3-1.4Ω

Not only has the new technology achieved breakthrough at reduced $R_{DS(on)}$ values, but new benchmarks have also been set for the device capacitances. A second effect to be considered in the switching losses is the energy being stored in the output capacitance. This energy E_{oss} (Figure 6) is transfered into heat during hard switched turn-on. Due to the strongly nonlinear voltage dependence of the output capacitance the 900V CoolMOS™ compensation devices offer here a very good performance if switched to more than 150V (marked in Figure 6).

Energy stored in the output capacitance of the MOSFETs is reduced by a factor of two or more at working voltage.

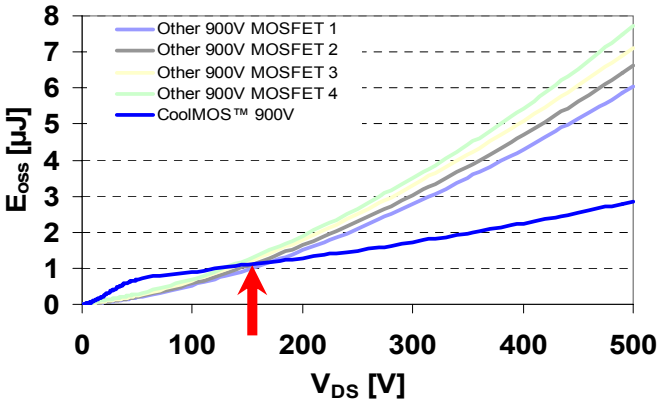

Figure 6 E_{oss} values for different 900V MOSFETs

3 Target applications CoolMOS™ 900V

The new CoolMOS™ 900V serie offers more design flexibility and pushes the existing limits towards higher power without significant disadvantages. Designers of power units benefit from the high blocking voltage, low $R_{DS(on)}$ and low Gate charge of the new CoolMOS™ 900V. Some examples are explained in the following paragraphs.

3.1 Wide range designs (90…270Vac) with their typical 400Vdc bulk voltage

Designs for standard grid voltages can benefit from the higher blocking voltage. Depending on the application the efficiency can be increased and/or design can be simplified without additional costs or other disadvantages.

Example 1: 500W Single Transistor Forward (STF) Converter used in ATX power supplies

Major benefits with CoolMOS™ 900V:

- **500W output power achievable with STF**
- **higher efficiency (+0.7% with BiC TO220)**
- **lower cost and part count**
- **easier design (no high side control)**

} **compared to TTF**

The output power benchmark for STF converters can be increased by using CoolMOS™ 900V. Up to 500W is achievable with a single MOSFET with increased performance and lower costs compared to standard Two-Transistor-Forward (TTF) with 200mΩ 500V/600V MOSFETs. Figure 7 shows the schematics of both topologies. In the STF we have only one transistor compared to the two transistors and the pulse transformer in a TTF.

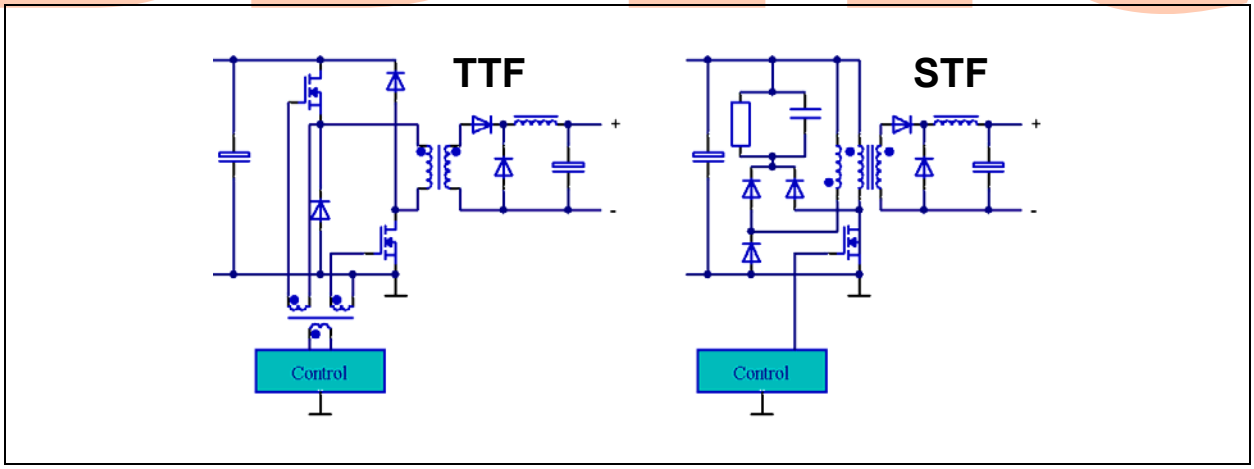

Figure 7 ATX power supplies (secondary side schematic being simplified).

Changing the topology from TTF to STF not only simplifies the design and adds layout benefits without the disadvantages (like the need of high-side-switching) of TTF.

Table 2 shows a comparison of the primary side losses of TTF and STF. Working frequency is 100kHz.

Table 2 Losses comparison Two-Transistor-Forward vs. Single-Transistor-Forward Converter

Losses	TTF with 200mΩ/600V	STF with 500mΩ/900V	STF with 340mΩ/900V
Conduction	6.5W	8.1W	5.5W
Output capacitance	2.8W	1.0W	2.1W
Switching	7.3W	4.7W	4.7W
Demagnetizing winding	---	0.5W	0.5W
Total losses	**16.6W**	**14.3W**	**12.8W**

Despite the higher $R_{DS(on)}$ of the CoolMOS™ 900V it is possible to design a STF with a higher efficiency than a TTF with 200mΩ 600V MOSFETs. This is due to the higher dynamic losses in a TTF because in every cycle two transistors have to be switched compared to only one transistor in a STF.

Indeed the transformer in a STF needs an additional demagnetizing winding which causes a small amount of losses which do not exist in TTF topology. But with careful design (bifilar winding) these losses can be very low and don´t influence the result significant.

Cost optimized designs use the 500mΩ CoolMOS™ 900V with slightly increased efficiency (compared to TTF with 200mΩ MOSFETs) and reducing losses up to 0.7% is possible using the 340mΩ CoolMOS™ 900V.

Example 2: 200W Quasiresonant Flyback converters for LCD-TV

Major benefits with CoolMOS™ 900V:

- **more than 200W of output power achievable with Quasi-Resonant Flyback**
- **improved EMI behavior due to true zero-voltage switching**
- **higher efficiency (+0.7% compared to 600V or 650V parts, 0.2% compared to 800V parts)**
- **lower voltage stress on secondary diodes or synchronous rectifiers**

Modern LCD-TV require output power up to 200W with high efficieny of the power supply together with low costs. The best topology for these requirements is the Quasi-Resonant Flyback Converter (QR-FB) and its disadvantages (like the high peak voltage on primary switch) are easy to handle with CoolMOS™ 900V.

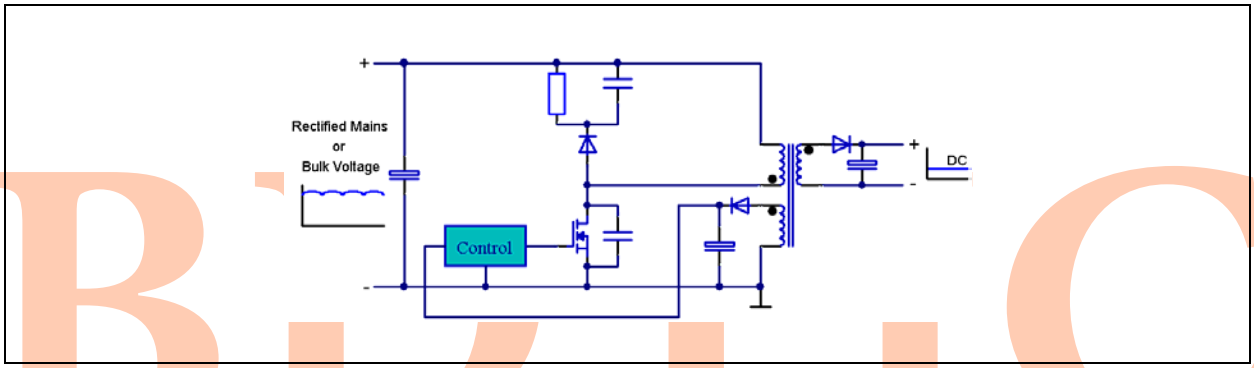

Figure 8 Quasi-Resonant Flyback Converter for LCD-TV (schematic simplified on secondary)

MOSFETs with high blocking voltage allow optimized transformer design resulting in reduced semiconductor losses and reduced voltage stress on secondary diode or synchronous rectifier.

Efficiency improvement of 0.2% compared to availabe 800V parts and even 0.7% compared to standard 650V parts is possible using CoolMOS™ 900V.

Table 3 shows the results of a 200W / 24V Quasiresonant Flyback design realized with 650V, 800V and 900V MOSFETs, respectively at a switching frequeny of 100kHz

Table 3 200W / 24V Quasiresonant Flyback with different types of MOSFETs

	650V 500mΩ CoolMOS	800V 500mΩ CoolMOS	900V 500mΩ CoolMOS	Benefit by using CoolMOS™ 900V
Duty Cycle at $V_{in,min}$ and max load	18%	27%	**32%**	Longer DC tue to higher reflected voltage
Peak current	4.8 A	3.1 A	**2.7 A**	Reduced peak current
Conduction losses	1.35 W	0.90W	**0.76 W**	Reduced conduction loss
Turn-on-losses	0.17 W	0.09 W	**0**	**True zero-voltage switching! → Improved EMI behaviour!**
Turn-off-losses	1.4 W	0.9 W	**0.8 W**	Reduced turn-off loss due to lower peak current
Voltage stress on secondary side diode	91 V	57V	**48V**	**Reduced voltage stress on sec. side diode or sync.rec MOSFET**
Total losses	6.6 W	5.6 W	**5.2 W**	
Efficiency loss	3.31 %	2.80 %	**2.61 %**	**Significant loss reduction! 0.7% vs. 650V 0.2% vs. 800V**

3.2 Replacement of IGBTs by CoolMOS™ 900V Series

Using a MOSFET with its Ohmic forward characteristic allow a significant reduction of conduction losses below the power dissipation of IGBTs where conduction losses can not fall below the on-set voltage times load current.

PFC and PWM stages are possible to up to 750V bulk voltage using CoolMOS™ 900V without diminishing safety margin.

Example 3: Renewable energy applications / solar converters

Major benefits with CoolMOS™ 900V:

- **more panels in series possible→lower copper losses in wiring**
- **higher overall efficiency**
- **no Overvoltage Protection (OVP) necessary**
- **smaller magnetic components due to higher switching frequency**

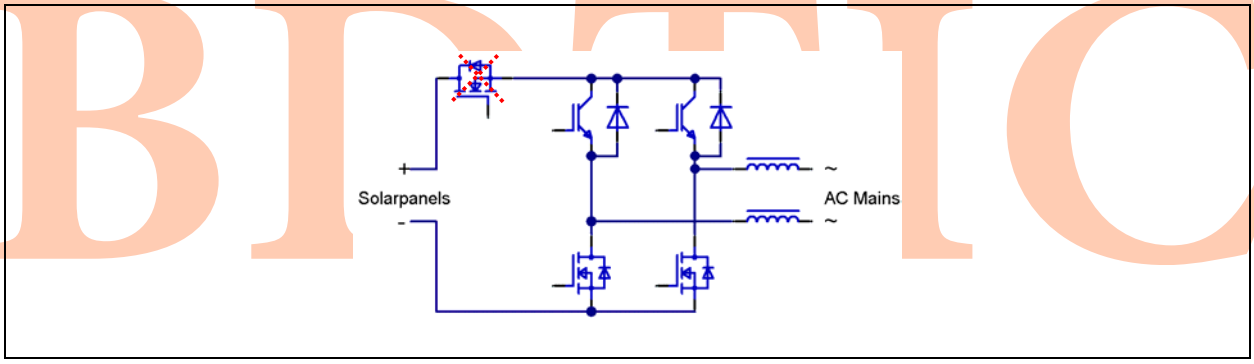

Figure 9 Typical DC / AC Solar Converter (with Overvoltage Protection)

Renewable energy applications such as photovoltaic converters show very high efficiency requirements due to system amortization via pay back of electricity fed back into the public network.

The use of MOSFETs instead of IGBTs enhances the efficiency especially in the mid range of output power - as being characteristic especially for many days in central and Northern Europe – by avoiding the characteristic onset voltage of the IGBT. The clear disadvantage of the MOSFET, its limited blocking voltage range and its more than square-law between $R_{DS(on)}$ and B_{VDSS} is amended by the new MOS generation CoolMOS™ 900 V. This new product family allows to build converters with an enlarged input voltage range coming thus closer to the upper limit of 1000 V as defined by the IEC 60364 for solar modules. Putting more panels in series instead of paralleling reduces significantly cabling losses, efforts and costs. Alone the cabling losses can be cut by factor of 2 when changing from 600 to 900 V voltage class.

Another factor in photovoltaic systems is size and cost of magnetic components. Offering a device with improved $R_{DS(on)}$ x Q_g and $R_{DS(on)}$ x E_{oss} performance allows an increase of switching frequency without suffering from the penalty of increased losses. Therefore reduction of system size is possible without losing energy efficiency.

3.3 Lighting applications

Using SEPIC topology as PFC converter eliminates high inrush current and improve surge current capability. With CoolMOS™ 900V the necessary higher blocking voltage compared to standard PFC boost topology can be handled.

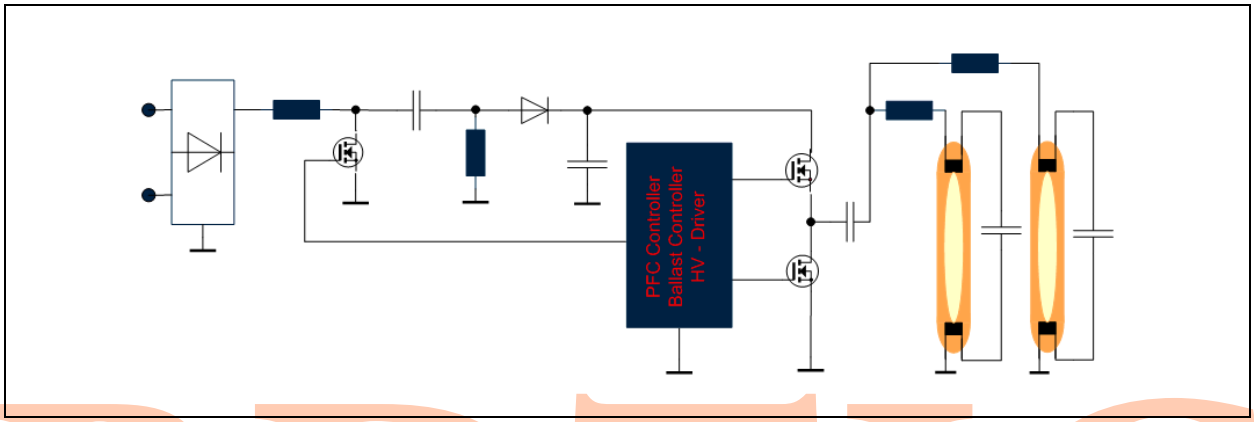

Figure 10 Lamp ballast with SEPIC preconverter

Additionally the 3-Phase-Supply of Lamp ballasts for street lighting and greenhouses requires a higher voltage capability than is offered with 600V or 800V MOSFETs, and lower on-resistance than what is offered with conventional 900V MOSFETs.

Ballasts for Flat Fluorescent Lamps require switches with a higher voltage capability due to the favored single switch resonant topology.

3.4 Auxiliary power supplies in 3-phase systems

Using a 3-phase grid the blocking voltage of the MOSFETs in auxiliary power supplies needs to be higher than 800V. With CoolMOS™ 900V Flyback converters even for higher output power levels are easy to design thanks to low conduction, switching and driving losses.

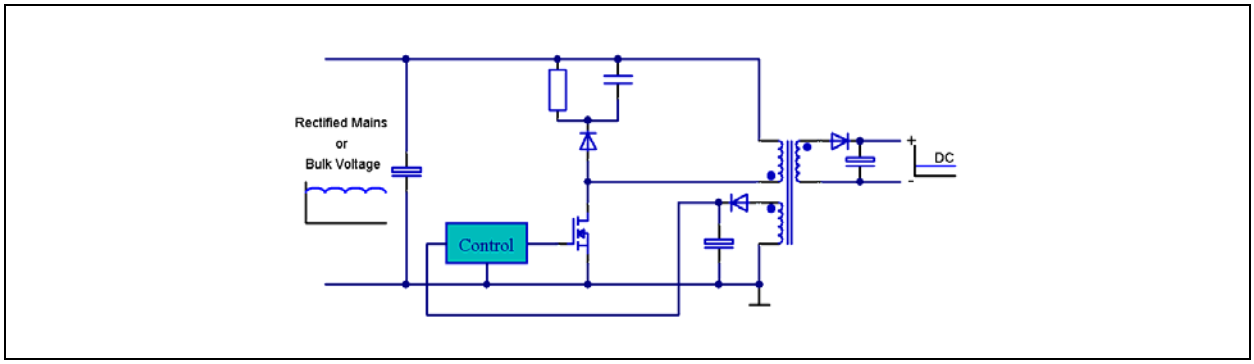

Figure 11 Flyback Converter for auxiliary power supplies

4 Product Portfolio

CoolMOS™ 900V portfolio in Figure 12 will be filled up during 2008.

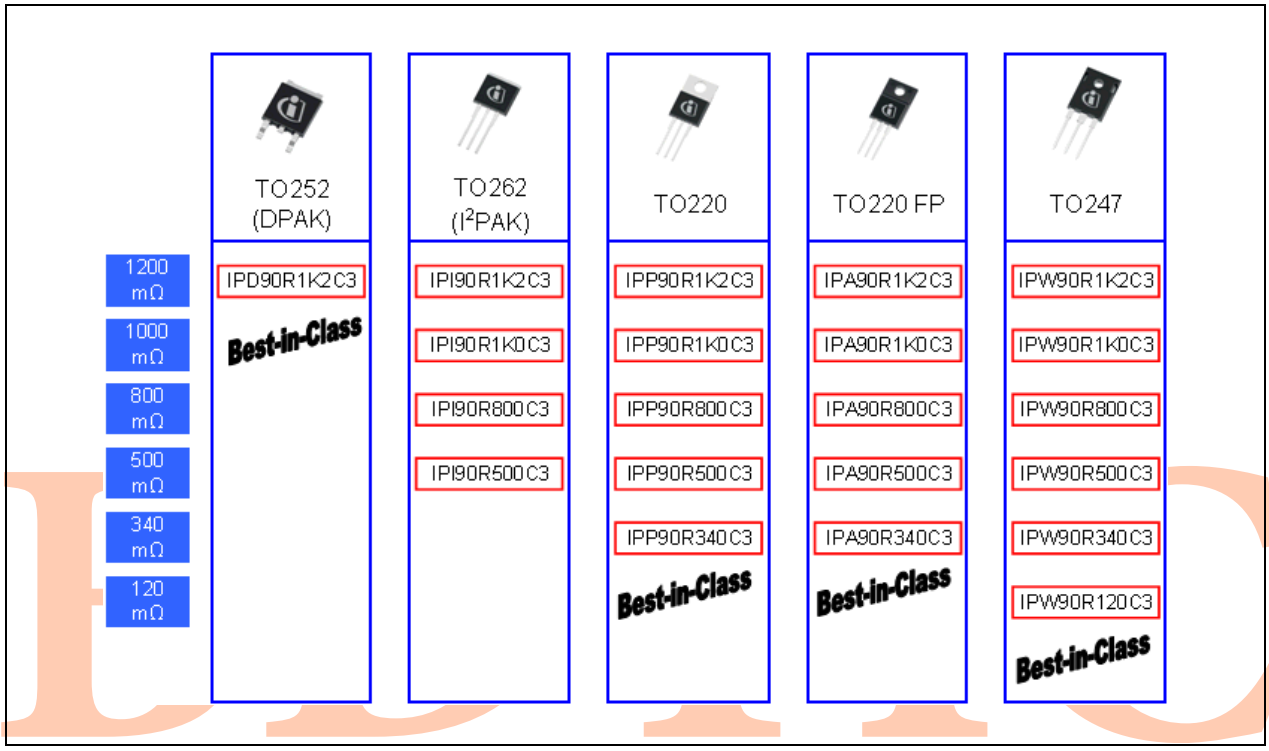

Figure 12 CoolMOS™ 900V Products.

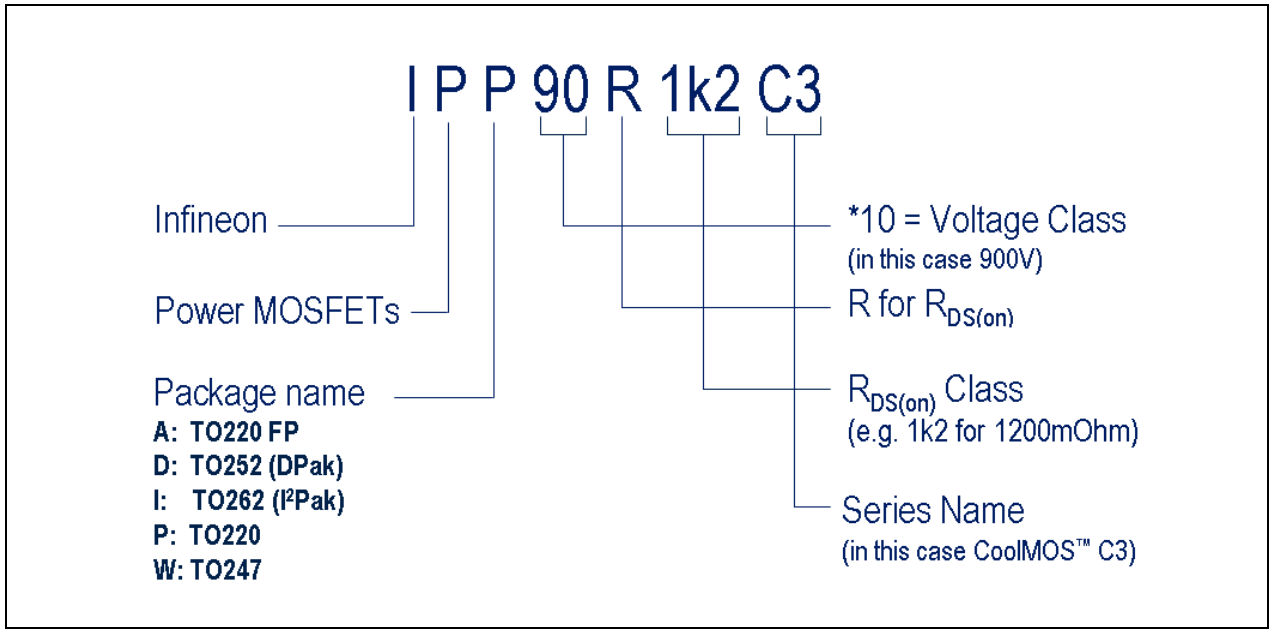

Figure 13 Naming System for CoolMOS™ Products

5 Circuit Design and Layout Recommendations

There are a number of recommendations to make with respect to circuit design and layout practices which will assure a combination of high performance and reliability. They can be recommended as if “in order of importance”, but realistically all are important, both in contribution toward circuit stability and reliability as well as overall efficiency and performance. They are not that dissimilar to recommendations made for the introduction of MOSFETs compared to bipolar transistors, or CoolMOS™ compared with standard MOSFETs; it is a matter of the degree of care.

5.1 Control dv/dt and di/dt by Proper Selection of Gate Resistor

In order to exert full R_g control on the device maximum turn-off dv/dt we recommend the following procedure:

1) Check for highest peak current in the application
2) Choose R_g accordingly not to exceed 50 V/ns (maximum rating in datasheet)
3) At normal operation condition quasi ZVS condition can be expected, which gives best efficiency results

5.2 Minimize Parasitic Gate-Drain Board Capacitance

Particularly care must be spent on the coupling capacitances between gate and drain traces on the PCB. As fast switching MOSFETs are capable to reach extremely high dv/dt values any coupling of the voltage rise at the drain into the gate circuit may disturb proper device control via the gate electrode. As the CoolMOS™ series reaches extremely low values of the internal C_{gd} capacitance (C_{rss} in datasheet), we recommend keeping layout coupling capacitances below the internal capacitance of the device to exert full device control via the gate circuit. Figure 14 shows a good example, where the gate and drain traces are either perpendicular to each other or go into different directions with virtually no overlap or paralleling to each other. A “bad“ layout example is shown as reference to the good layout in Figure 15.

If possible, use source foils or ground-plane to shield the gate from the drain connection.

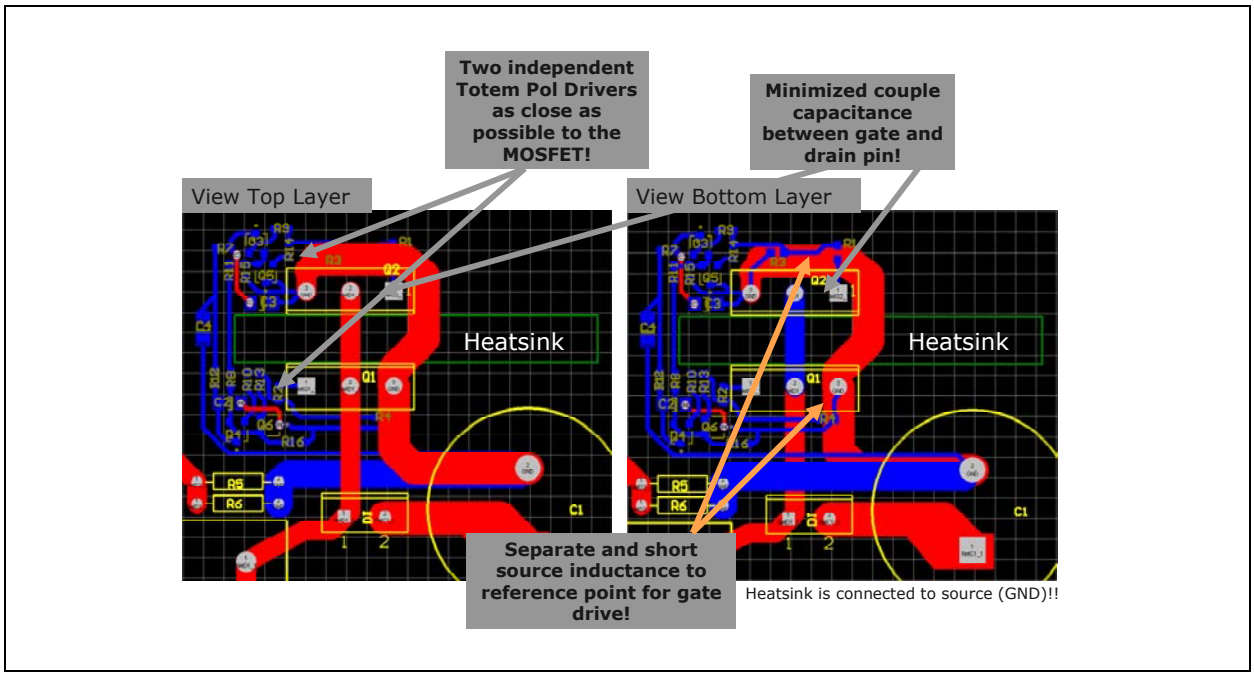

Figure 14 Good Layout Example Ensuring Clean Waveforms When Designing in CoolMOS™

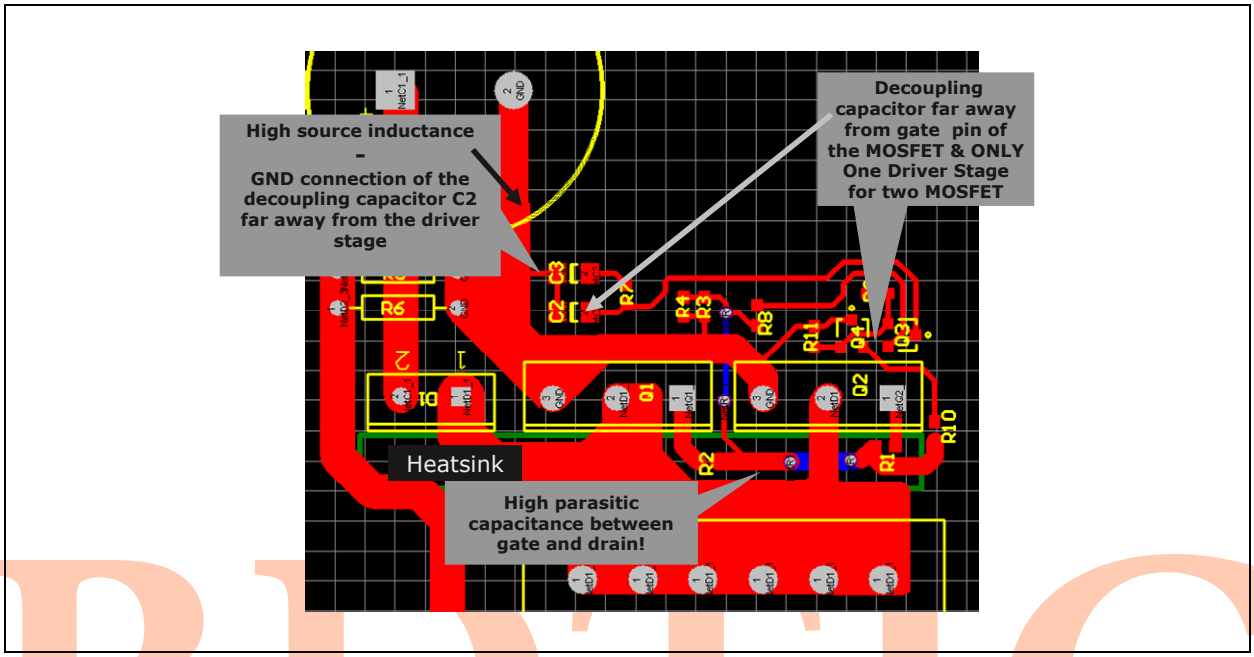

Figure 15 Bad Layout Example

5.3 Locate Gate Drivers and Gate Turn-Off Components as Close as Possible to the Gate

Always locate the gate drive as close as possible to the driven MOSFET and the gate resistor in close proximity of the gate pin. This prevents it acting as an antenna for capacitively coupled signals. The controller/IC driver should be capable of providing a strong “low” level drive with voltage as near to ground as possible- MOS or bipolar/MOS composite output stages work well in that regard, due to low output saturation voltages. While some drivers may be deemed to have sufficient margin under static or “DC” conditions, with ground bounce, source inductance drop, etc, the operating margin to assure “off” mode can quickly disappear.

5.4 Use Symmetrical Layout for Paralleling MOSFETs, and Good Isolation of Gate Drive between FETs

We recommend the use of multi-channel gate drivers in order to have separate channels for each MOSFET. Physical layout should be as symmetrical as possible, with the low impedance driver located as close as possible to the MOSFETs and on a symmetric axis.

5.5 Summary

To summarize, below recommendations are important when designing in CoolMOS™ 900V to reach highest efficiency with clean waveforms and low EMI stress.

- ✓ Control dv/dt and di/dt by proper selection of gate resistor
- ✓ Minimize parasitic gate-drain capacitance on board
- ✓ Locate gate drivers and gate turn-off components as close as possible to the gate
- ✓ Use symmetrical layout for paralleling

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